PI74FCT162344T for Heavy Load Applications

Introduction

Complex memory modules and high-end motherboards require a driver to buffer and drive many loads. Often, the total capacitative load for each load may exceed 150pF. As a result, the driver propagation delay significantly increases and the signal waveform deteriorates as it travels down the trace. This brief describes the PI74FCT162344T advantages in heavy load applications.

Enhanced Driving of Transmission Lines

On high-performance motherboards, the signal rise/fall times are extremely fast, undermining signal integrity. Figure 1 shows a typical FCT16244 buffer driving 12 logic devices. Since most traces on the board must be treated as transmission lines, this loading condition causes signal integrity to deteriorate even more.

On the other hand, the PI74FCT162344T has far greater fanout. Its output stage was designed for balanced a drive (both rise and fall directions). The I/V curve indicates ±24mA static current. Actually the available instantaneous current is 150mA which allows for driving high capacitance loads. Figure 2 exhibits each of the 4 outputs driving only 3 loads instead of all 12...this is a **major advantage.** Thus the Address/Clock Driver devices offer a solution for converting heavy loads to light loads.

Maintaining Low Skew

Because there are twice as many output drivers on the FCT162344, 32 to 16 on the FCT16244, skew between drivers becomes very important. Skew is typically 0.25ns (see data sheet for exact specification method). Figure 2 exhibits this skew. It should be noted that trace length matching is also extremely important. Typically propagation delay is 0.2ns per inch of trace. If traces are mismatched by 1 inch, this would result in a skew error of 200ps.

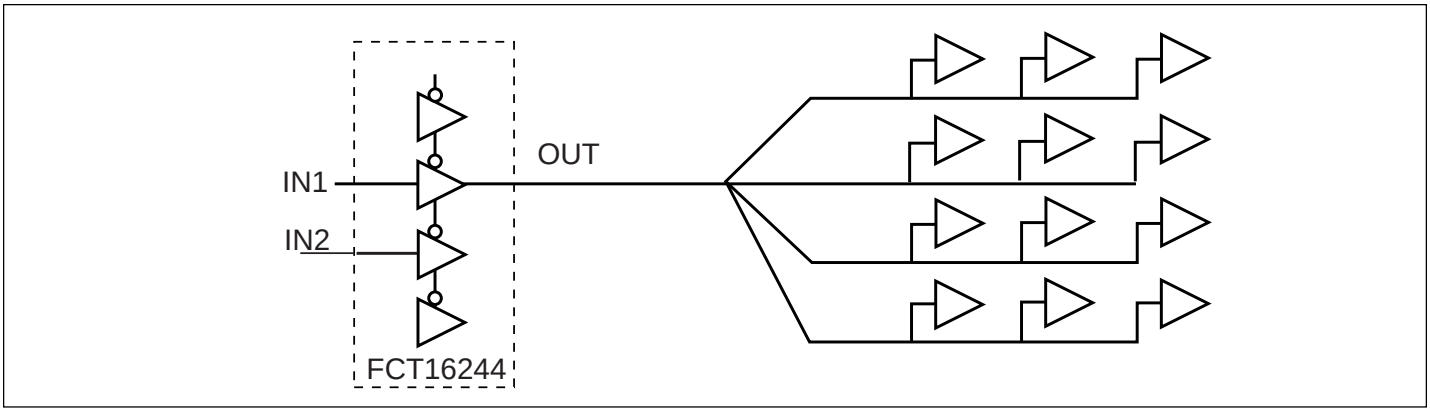


Figure 1. Driver With Heavy Loads

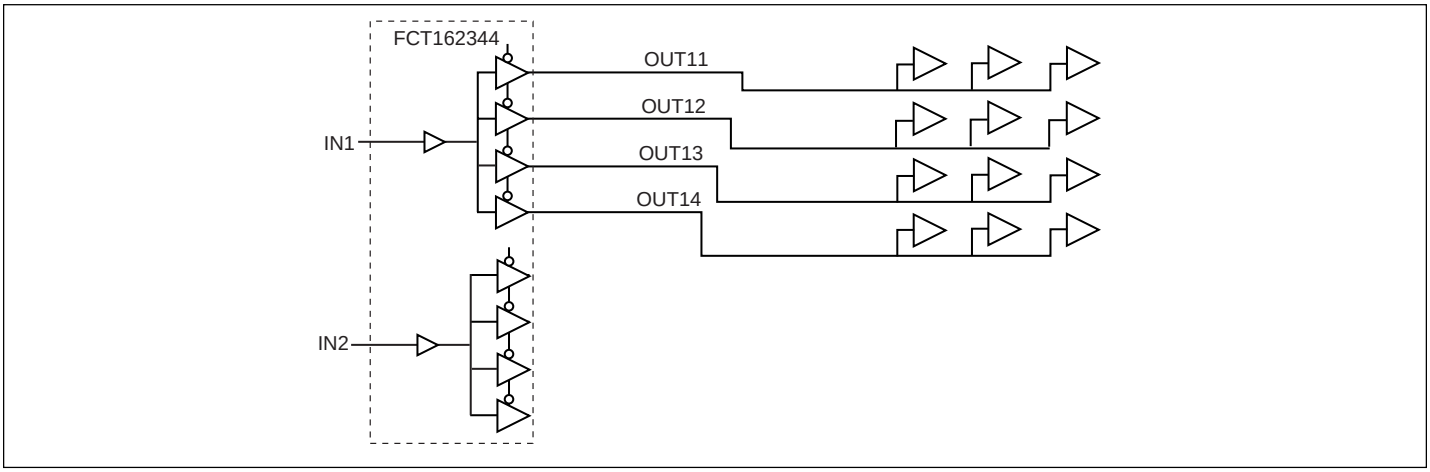


Figure 2. Improved Solution - Driver With Nominal Loads

Product Features

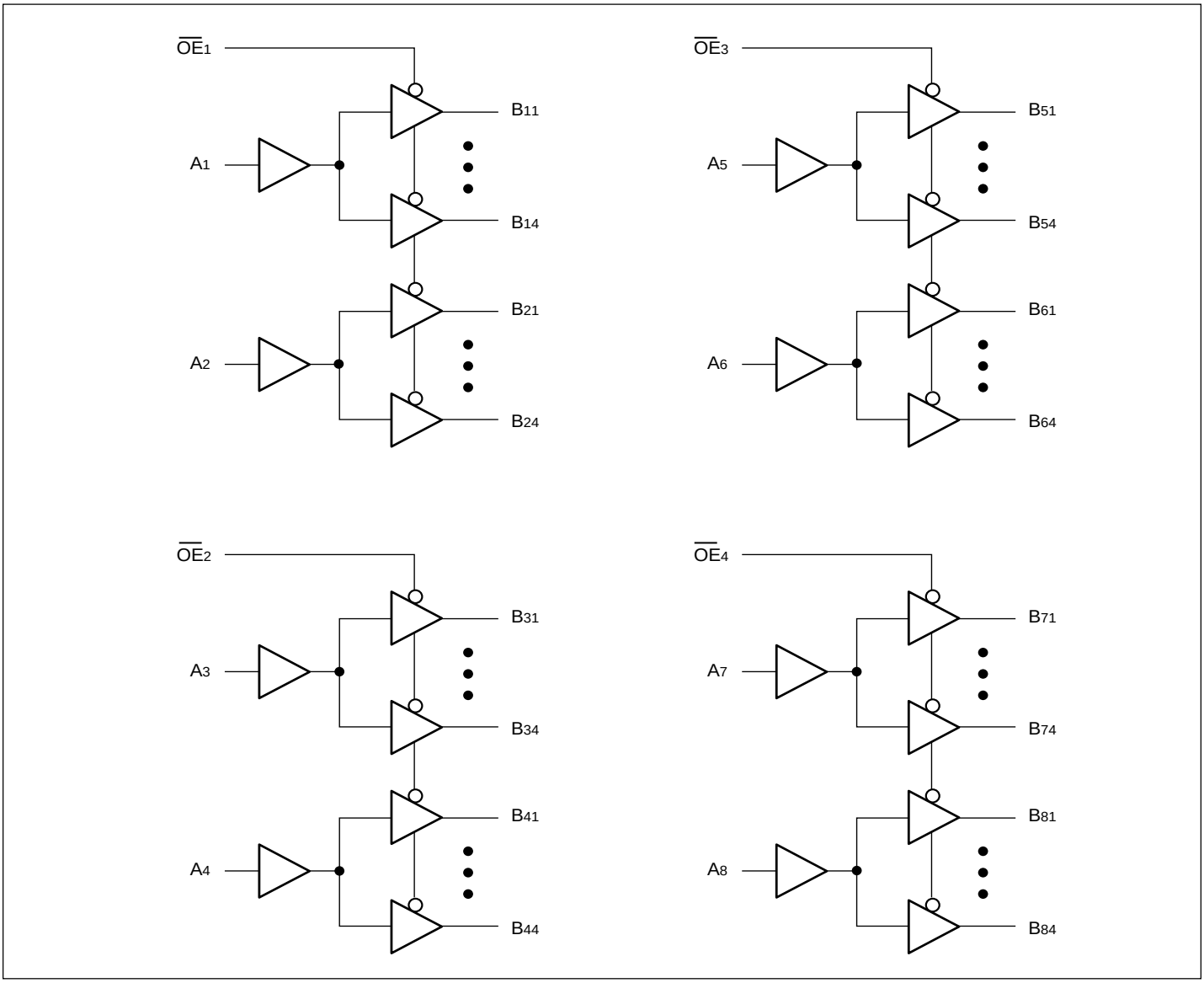
- Ideal for address line driving and clock distribution
- Eight banks with 1:4 fanout with 3-State control
- Typical tsk(o) output skew < 250ps
- Propagation Delay: 3.8ns Max
- Balanced output drivers: ±24mA
- Hysteresis on all inputs
- Packages available:
  - 56-pin 240-mil wide plastic TSSOP (A56)
  - 56-pin 3000-mil wide plastic SSOP (V56)

Product Description

Pericom Semiconductor's PI7FCT series of logic circuits are produced using the company's advanced 0.6 micron CMOS technology to achieve industry leading speed grades. The PI74FCT162344T is an address/clock driver designed to provide fanout to memory arrays. Eight banks, each with a fanout of four, and 3-state control, provide efficient address distribution. One or more banks may be used for clock distribution.

The PI74FCT162344T has balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



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