The Behavior of CMOS in Hot Insertion

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PMOS, as half of the CMOS, is commonly used in logic and switch devices. Also, PMOS is commonly used as a pull-up resistor along with many other elements in an integrated circuit.

This study will analyze the phenomenon and mechanism of the problem caused by PMOS during hot insertion for logic driver, CMOS switch, and PMOS pull-up resistor.

What happened during hot insertion?

During hot insertion, the system and circuit condition is as follows (see Figures 1, 2, 3 on next pages)

- The grounds of the insertion card and the back plane will connect before any other pins (this is the industry standard request for hot insertion).
- The power from the backplane will ramp up slowly (at ns level) due to the time delay caused by the bypass capacitors at the DC/DC power converter on the insertion card.
- A signal from the backplane will apply to the PMOS (in the CMOS driver or in the CMOS switch) directly and without delay (at ns level), while the V_{CC} supplied to the chip on the card is 0V (due to the power delay mentioned above).
- The hot insertion condition above can be summarized as that the 3.3V signal from the backplane applied to the chip, while the voltage at the V_{CC} pin of the chip is 0V.

PMOS sinks signal from backplane with two paths

- Path One: The 3.3V signal from the backplane will be forwarded to the ground through the PN junction (0.7V), the bulk terminal B, the V_{CC} pin of the chip (0V), and the bypass capacitor. See Figure 1 for the example of CMOS driver.
- Path Two: When the signal from the backplane is 1.1V higher than the 0V at gate and source, the signal voltage is higher than the 1.1V threshold of the PMOS, thereby will turn the P-channel on. See Figure 1 for the example of CMOS driver.

When the PN junction is clamping the signal from the backplane at 0.7V, the signal voltage at drain is lower than the 1.1V threshold of PMOS, thereby the P-channel will be off. The P-channel can be turned on only when path-one is de-conducted, thereby the voltage at drain can reach the 1.1V threshold of the PMOS and turn the PMOS on.

Figure 1 shows the hot insertion condition at transistor structure level. Figure 2 and 3 show the hot insertion condition for logic driver and CMOS switch at device level.

NMOS, the another half of the CMOS, will not sink the signal from the backplane, neither by its PN junction nor its N-channel during hot insertion. See Figure 4.

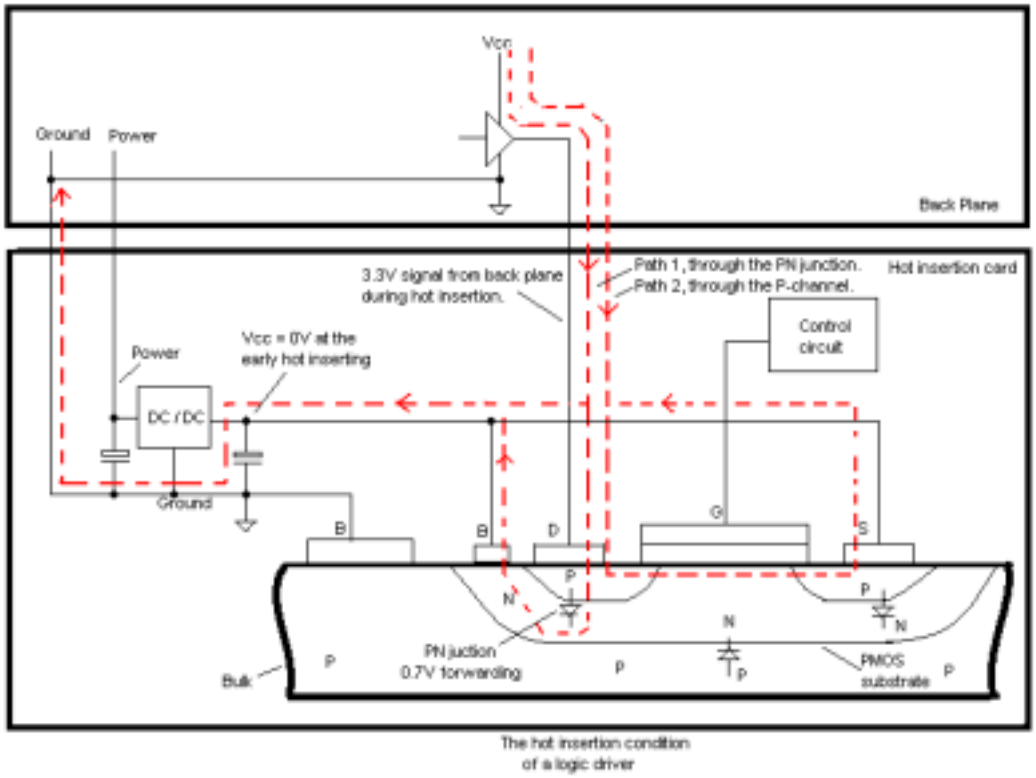

Figure 1. The hot insertion condition at transistor structure level

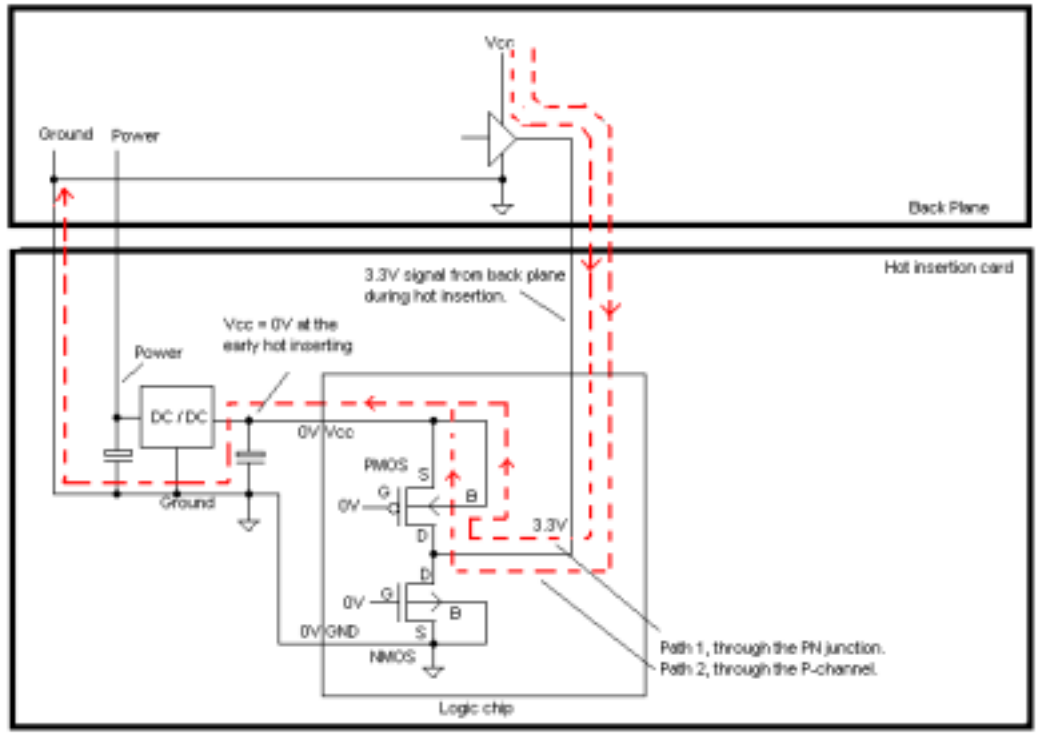

Figure 2. The hot insertion condition for a CMOS driver

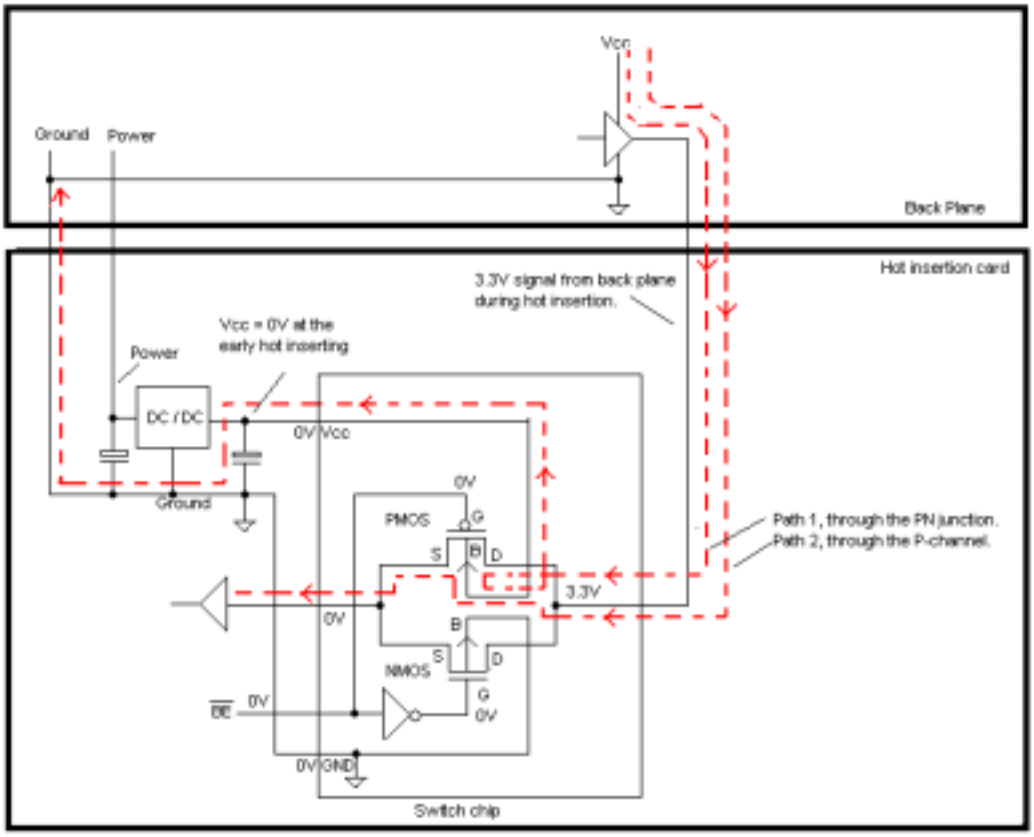

Figure 3. The hot insertion condition for a CMOS switch

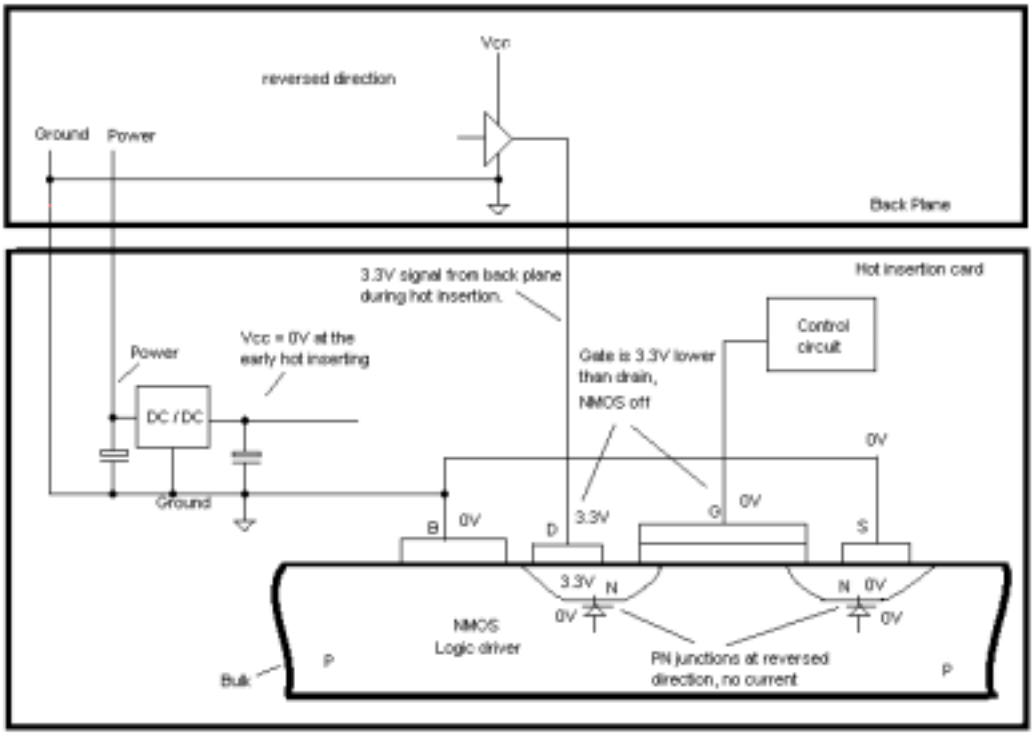

Figure 4. The NMOS will not sink the signal from the backplane, neither by its PN junction, nor its N-channel during hot insertion