Interface single-ended signal to DDR devices

By Paul Li

Introduction

Today's Gigahertz CPUs request high bandwidth on the PC board. The TTL signal on the board becomes the bottleneck since the maximum frequency of TTL signals traveling through the PC board is less than 200 MHz.

The large amplitude of TTL signals take a longer time to swing between rails, and the high capacitance associated with TTL signals parallel the bus structure attenuating the edges of TTL signal tremendously, while limiting the maximum speed. TTL signals also consume high power at high speed due to wide signal swing and high capacitance.

Differential receivers can reject common noise and therefore are capable of working at smaller amplitude at higher speed. Differential signals have much lower capacitance due to their point-to-point (non-bus) structure. Thus, at low swing range and capacitance, differential signals can work at a much higher speed with low power consumption. The DDR clock also benefits from double data rate, because they use every edge as a clock.

Therefore, differential signals, including DDR signals, are commonly implemented in IC chips such as ASICs, clock, DRAM devices, and gradually dominating the PC board design, while traditional TTL devices still remain. System designers are now facing the task of interfacing the DDR devices with conventional single-ended signals.

This article is intended to provide design guidelines of interfacing DDR devices with single-ended signals.

Single-ended signal to DDR

The interface circuit in Figure 1 shows an example of interfacing a single-ended signal to a DDR device using a common DDR PLL-clock buffer 855.

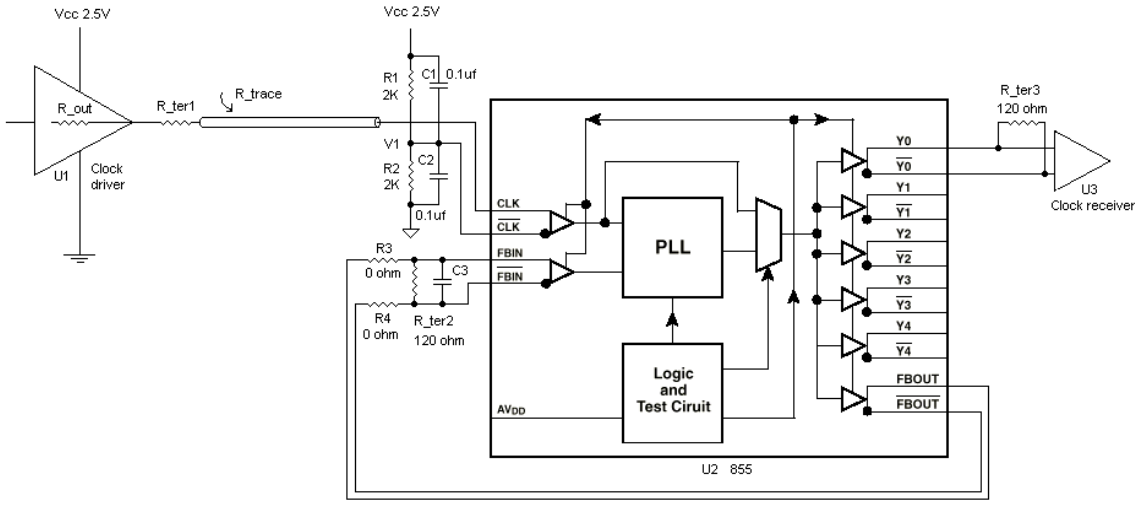

Figure 1: The circuit of interfacing single-ended signal to DDR

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Circuit analysis and adjustment

Matching the trace impedance

In Figure 1, the series resistor R_ter1 is a termination resistor used to match the impedance of the trace between clock driver U1 and the DDR receiver U2. Signals at a trace with well-matched impedance will form an "ideal" shape of rising and falling edges at end of trace. There will be no overshoot, undershoot, nor significant attenuation on the edges if conditions are that the capacitive load is slight. Transmission line theory shows that the impedance of a trace is matched when: R_out + R_ter1 = R_trace

Where:
R_out: The output impedance of the clock driver U1, it is normally in the range of 8-ohm to 45-ohm.
R_ter1: The series termination resistor, it is normally in the range of 0-ohm to 40-ohm. It should be deployed at the output pin as close as possible.
R_trace: The impedance of the trace between clock driver U1 and DDR clock U2, the impedance of the trace is controlled by the trace parameters and PCB fabrication processing, normally in the range of 50-ohm to 60-ohm.

For instance, if the driver's output impedance R_out is 30-ohm, and the trace impedance R_trace is 50-ohm, then:
30-ohm + R_ter1 = 50-ohm
R_ter1 = 20-ohm

The impedance of the trace is matched when R_ter1 is 20-ohm.

Reflection effect and RC effect

There are two phenomenons' that will affect the shape of the reflected waveform at the end of a trace: The transmission line reflection effect and the RC effect.

The reflection effect

The impedance of a trace will be matched when (R_out + R_ter1) = R_trace and the reflection at end of the trace will form a "perfect" waveform, it is rail-to-rail without overshoot, undershoot, nor edge attenuation (see Block A in Figure 2).
Overshoot and undershoot will be seen proportionally when: (R_out + R_ter1) < R_trace; edge attenuation will be seen proportionally when: (R_out + R_ter1) > R_trace (see Blocks B and C).

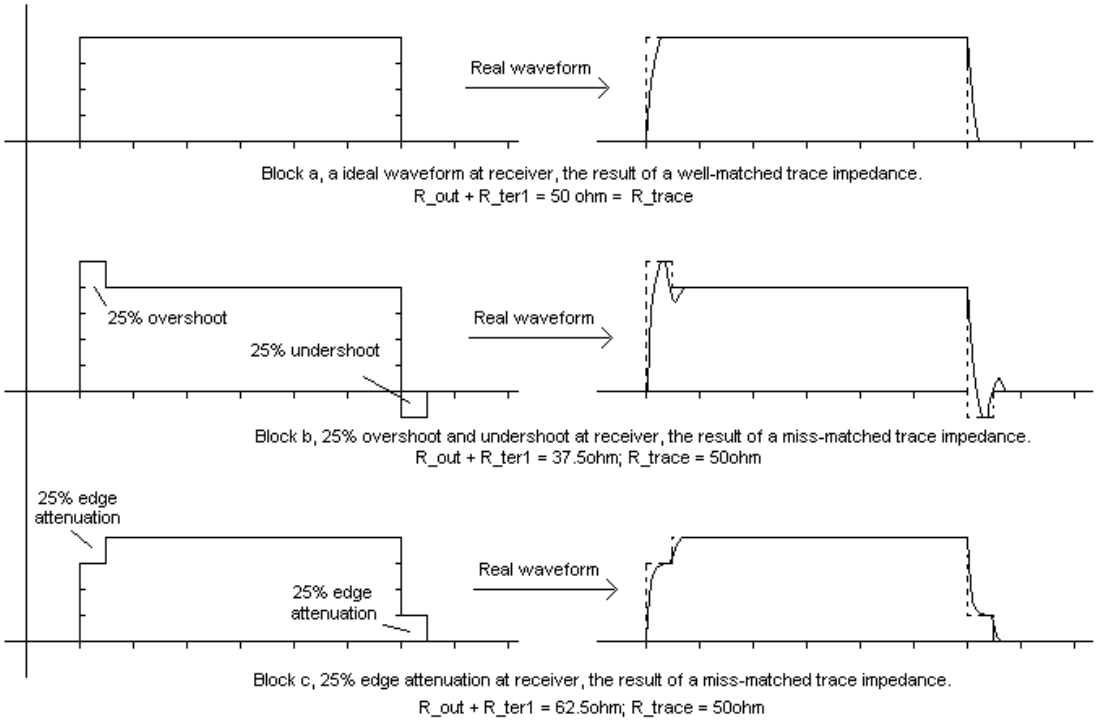

Figure 2: The waveforms at the end of a trace formed by reflection effect

The RC effect

The RC effect is the result of the RC circuit consisting of R_out, R_ter1, trace capacitance, and the capacitance of the DDR receiver. When the capacitive load is higher than 40pf, the RC effect slows down the edges and overrides the overshoot, undershoot, and attenuation (see Figure 3).

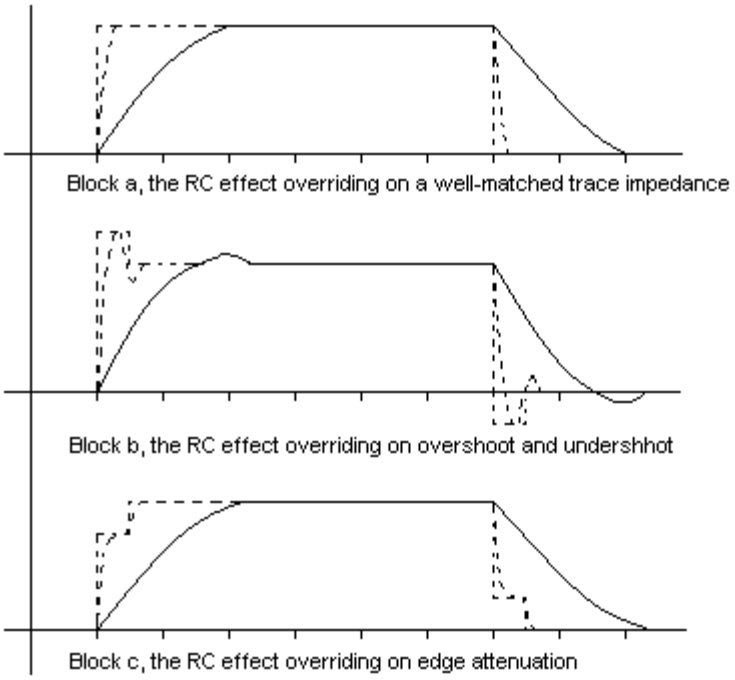

Figure 3: The RC effect

The Domination: Reflection Effect versus RC Effect

Reflection effect determines the shape of waveforms at the end of traces when the capacitive load is less than 20pf, and frequency is below 200 MHz. In such a condition, matching the impedance is essential.

RC effect dominates the shape of waveforms when the capacitive load is higher than 40pf, and will slow down the edges of signals significantly.

Therefore, when matching the trace with heavy capacitance such as a bus structure and long trace or cable, properly reducing the output impedance from the matching value is a common approach to compensate the loss of RC effect, especially in a bus structure. IBIS model simulations are a good tool to help in a system designer's signal integrity analysis.

At frequencies higher than 500 MHz, the reactance of a capacitive load is much lower and will attenuate the signal tremendously. Therefore, the major request for a high-speed circuit design is low capacitive load (less than 10pf at 500 MHz), then matching the impedance. The low capacitance associated with point-to-point structure of a differential signal is one of the main reasons why the differential signal is dominating the PCB design.

Adjust the feedback delay to optimize the system clock timing

The feedback loop is the trace and circuit between FBOUT and FBIN (see Figure 1). The main feature of a PLL clock compared with a non-PLL clock buffer is the ability of adjusting the system clock timing through altering of the feedback time delay. The timing relationship between clock input, clock output and feedback loop is shown in Figure 4.

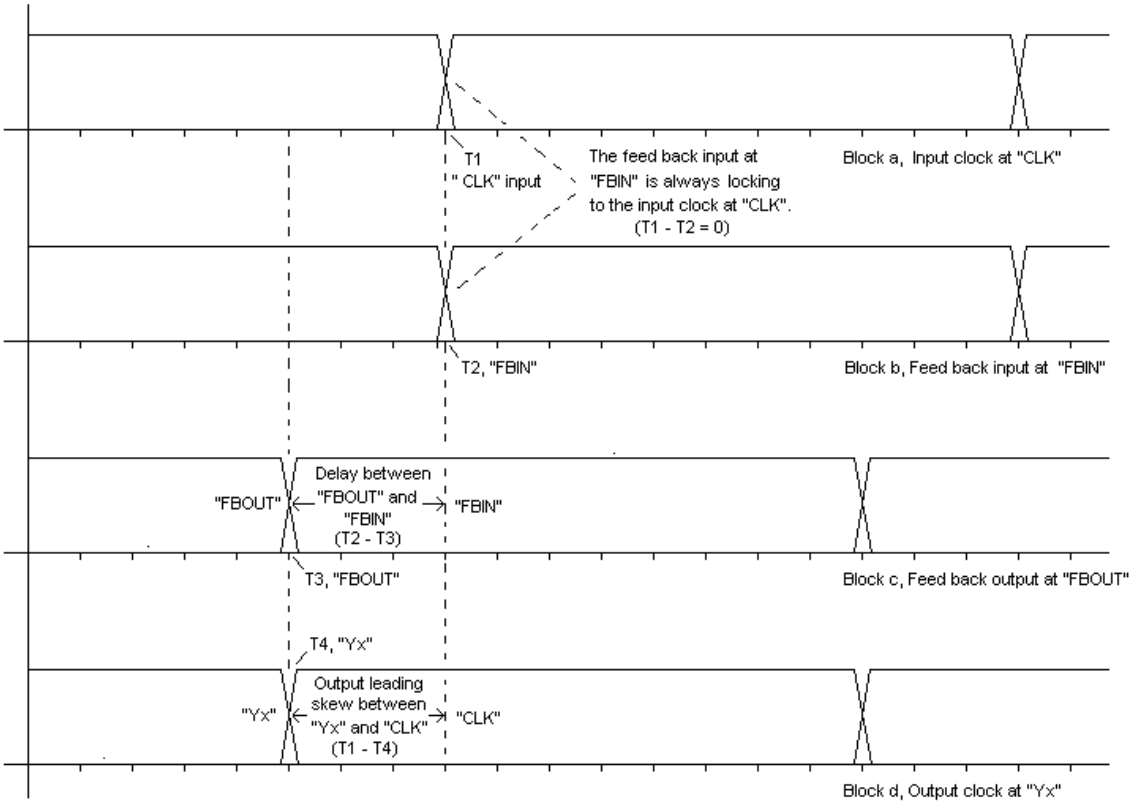

Figure 4: The timing relation between clock input, output and feedback loop (refer to Figure 1)

The following is the mechanism of generating a leading or lagging skew (refer to Figures 1 and 4):

- The feedback edges of "FBIN" at T2 is always chasing and locking into the clock input edges at "CLK" at time T1 (see blocks A and B). As long as the PLL is functioning, the time difference between T1 and T2 is zero (T1 - T2 = 0). This is the principle mechanism of why the PLL can generate a precise output leading skew (the output is earlier than the input), or lagging skew.
- The feedback delay between FBOUT and FBIN (T2 - T3) generates the same amount of output leading skew between "Yx" and "CLK" (T1 – T4) respectively. This is because the drivers of "FBOUT" and "Yx" are identical and are connected to the same input. As long as the PLL is functioning, we will always have (T2 - T3) = (T2 – T4). Since T1 = T2, we have (T2 - T3) = (T1 – T4).
- Thus, by varying the time delay between "FBOUT" and "FBIN" (T2 - T3), we can generate the same amount of output leading skew (T1 – T4) at "Yx".

For instance, when the feedback delay between FBOUT and FBIN (T2 - T3) is zero, the output skew between "Yx" and "CLK" (T1 – T4) should be zero. If the feedback delay is 1.2ns, there will be a 1.2ns leading skew at "Yx", and the output edges at "Yx" is 1.2ns earlier than the edges at "CLK".

The feature of generating leading skew is a very useful for a PLL DDR clock; it provides the approach of system clock timing adjustments.

Feedback delay generated by trace and RC circuit

- 70% to 85% of the feedback delay (T2 – T3) should be generated by the delay of the trace in feedback loop (Figure 5). The speed of a signal traveling in a trace is 50% to 70% of the speed of light, which is approximately 6 to 8 inches per nano-second, depending on the type and parameter of the trace. The purpose of the 70% to 85% time delay generated by the trace is to provide a stable time base. A non-connected second pair of traces at different lengths is also commonly deployed on the PC board for a spare timing option (Figure 5). The second pair of trace can be jump-connected to the feedback loop through pads in case the first pair of trace is disconnected due to its timing not being suitable after the PC board is fabricated.
- 15% to 30% of the feedback time delay should be generated by the RC circuit consisting of R3, R4, C3, and the input capacitance of "FBIN". The purpose of the 15% to 30% delay generated by the RC circuit is to provide the flexibility of fine-tuning.
- Fine-tuning the values of R3, R4, R_ter2 and C3 after the fabrication of the PCB will provide accurate system clock timing. R_total (R3 + R4 + R_ter2) is specified at 120ohm as default. Adding resistance from 0ohm to 22ohm to R3 and R4 while keeping the R_total at 120ohm will add extra feedback delay due to the RC delay consisted of R3, R4 and the input capacitance of FBIN (and C3, if any). C3 is defaulted at 0pf because capacitance slows down the slew rate, which is not preferred. Adding capacitance from 2pf to 10pf to C3 will generate more feedback delay. Reducing the entire R_total will reduce the peak-to-peak swing range and the signal will swing faster at smaller range therefore the feedback delay will be decreased, vice versa.
- If the lengths of the output traces at output of "Yx" are not equal while equal clock timings are requested, matching up the shorter traces with the longest trace with extra dummy routing.

For instance, in Figure 5, there is a 1.2ns trace delay between "Y0" (T4) and U3 (T5). In case we want a zero delay between "CLK" and U3, we need the "Y0" to be 1.2ns earlier than "CLK" (T1) to compensate for the trace delay between "Y0" and U3. Therefore, we need a 1.2ns feedback delay between "FBOUT" and "FBIN" (T2 – T3). Please refer to Figure 6 for a detailed timing relation.
In this example, 75% (0.9ns) of the 1.2ns feedback delay is generated by the feedback trace and 25% (0.3ns) is generated by the RC circuit consisting of R3, R4, R_ter2, C3, and the input capacitance of "FBIN".

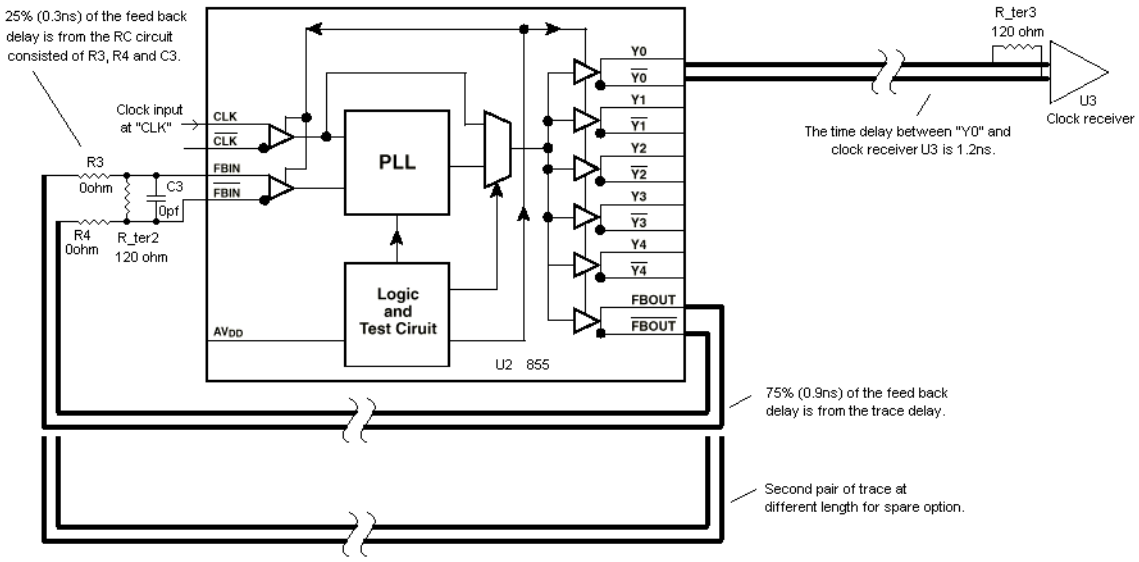

Figure 5: Example of the feedback loop delay

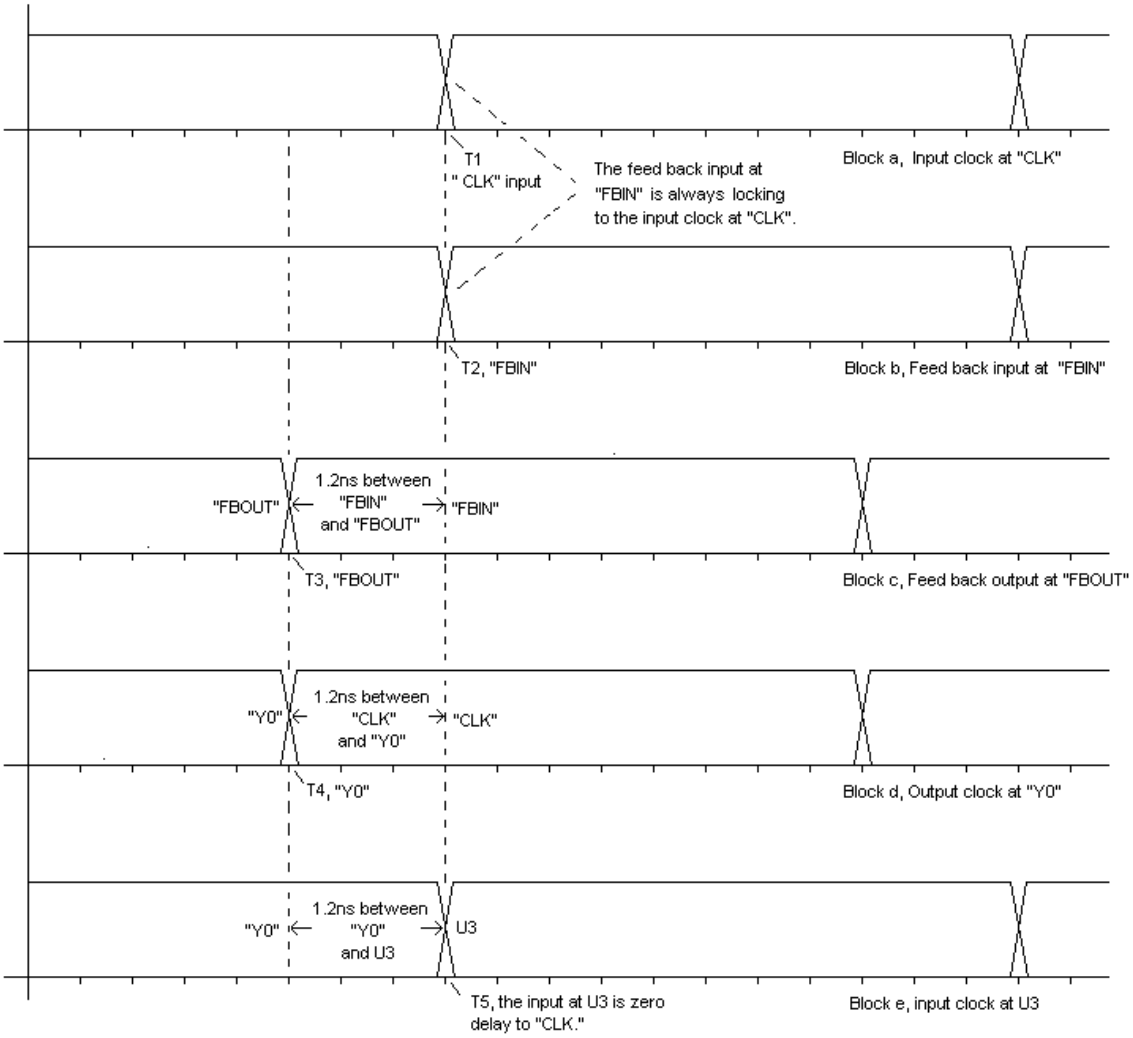

Figure 6: The timing relation between clock input, output, feedback delay and clock receiver U3

Interfacing 3.3V and 5V single-ended signal to DDR

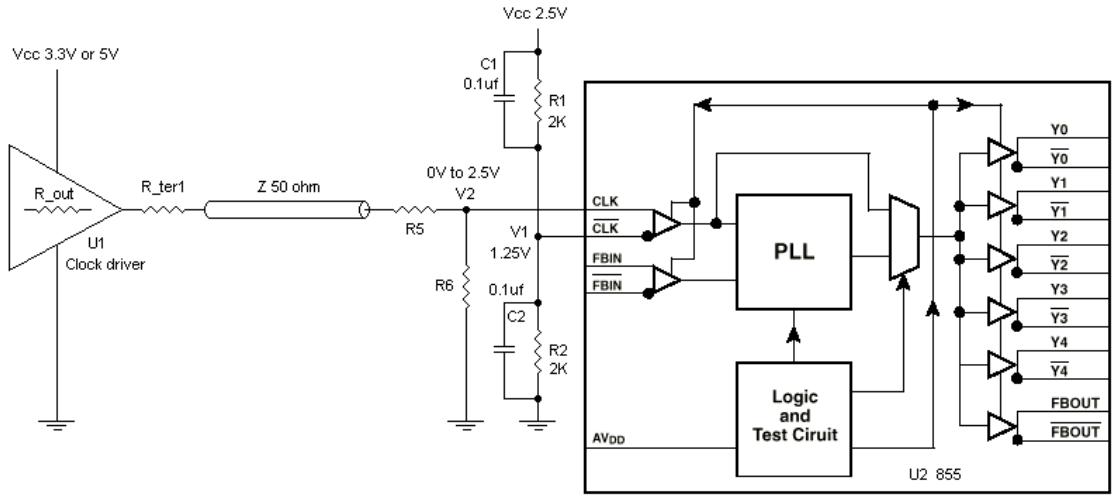

Figure 7: The interface circuit for 3.3V and 5V single-ended signals to DDR

When 3.3V and 5V single-ended CMOS drivers are connected to a DDR receiver, using the circuit in figure 7 and the values in Table 1, fine-tuning R5 for a 0V to 2.5V swing at V2. The value of R_ter1 is from 0-ohm to 15-ohm: increasing R_ter1 if overshoot and undershoot is seen at V2 and reducing R_ter1 if signal attenuated.

Table 1: The values of R3 and R4

Part number	For 3.3V input signal	For 5V input signal
R5	30-ohm	125-ohm
R6	125-ohm	130-ohm

DDR to Single-ended signal

Any single output of the DDR output pair could be used as a 2.5V single-ended clock driver, driving a 2.5V clock receiver.

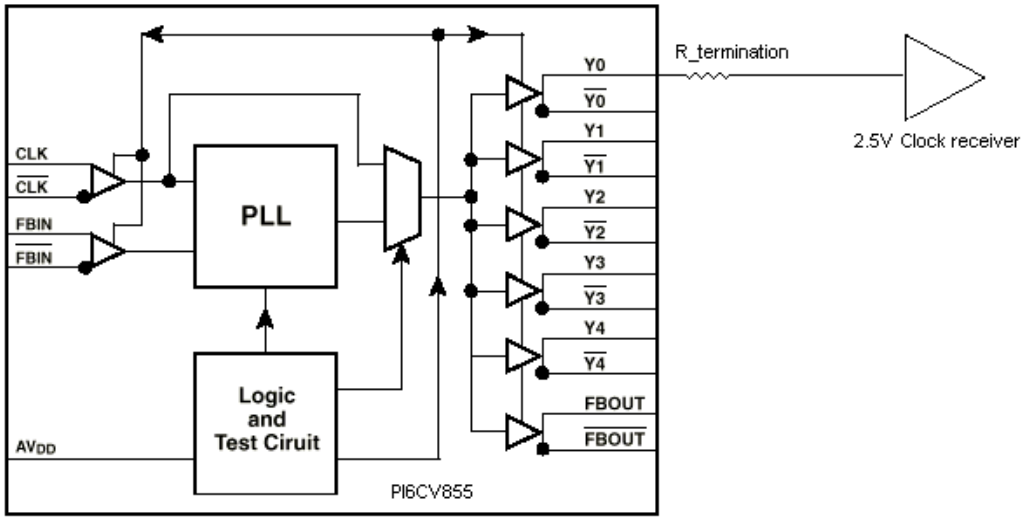

Figure 10: Interface DDR output to a 2.5V single-ended clock receiver

The adjustment of duty cycle balance

DDR standards require much more precise tolerance for duty cycle balance than a normal TTL signal. Thus, the duty cycle balance of the DDR output of a non-PLL DDR buffer (Figure 8) needs to be adjusted when interfaced to a single-ended input signal.
A DDR PLL clock-buffer does not have the duty cycle balance issue because a DDR PLL clock-buffer is a PLL device, its feedback is only locking to the input rising edge at "+CLK" and ignores the duty cycle of the input signal. Therefore, its output duty cycle is dependent on the internal duty cycle balance circuit and can not be adjusted externally.

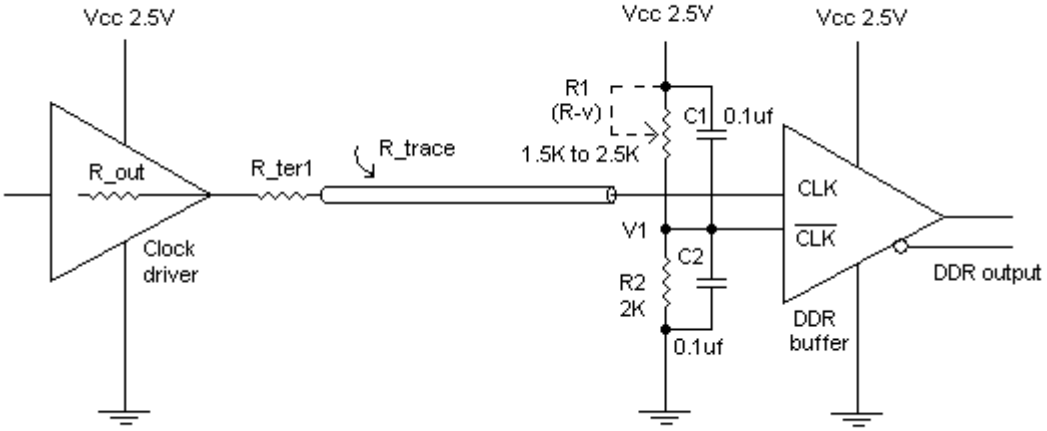

Figure 8: The circuit of duty cycle adjustment for a non-PLL buffer

In Figure 8, V1 is determined by the voltage divider consisting of R1 and R2. Normally, V1 = Vcc/2 = 1.25V. Adjusting the voltage of V1 can improve the duty cycle of the output clock (see Figure 9). The preferred value of R1, or R2 is from 1K to 5K: Lower resistance will cause higher DC current but better noise immunity and vice versa.
Fine-tuning R-v (R1) to adjust V1 according to Figure 9 will improve the output clock's duty cycle.
V1 = Vcc □ {R2 / (R1 + R2)}

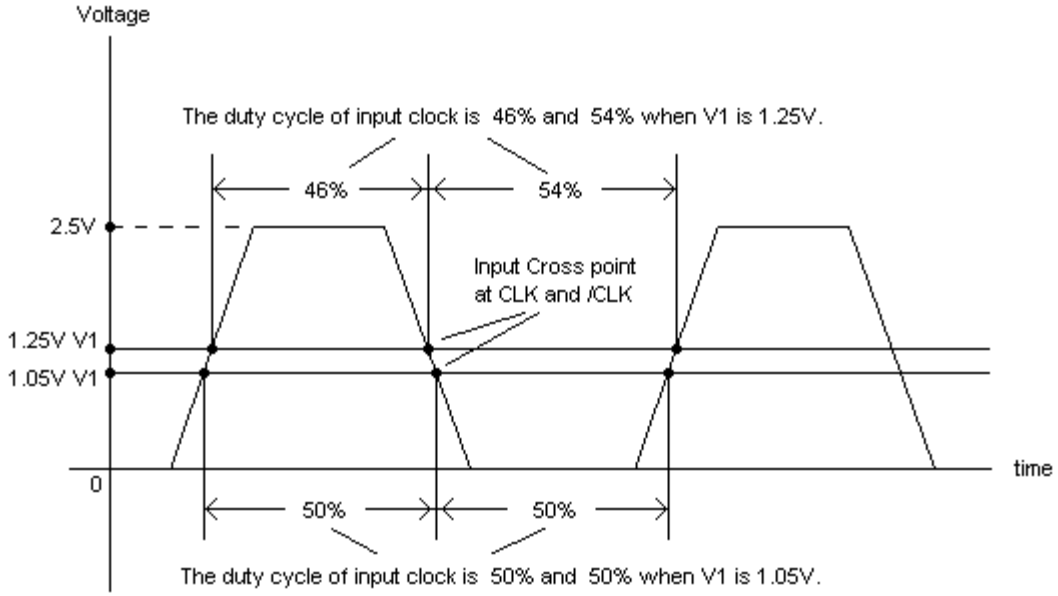

Figure 9: Adjusting V1 for better DDR clock output duty cycle

When adjusting the output clock's duty cycle, fix the resistance of R2 (e.g. at 2K); replace R1 with a 3K variable resistor R-v. Then, measure the cross points of the DDR output clock's duty cycle at "+Y0" and "-Y0" using two probes while adjusting R-v until the output duty cycle is balanced. Carefully selecting the single-ended signal driver with good duty cycle (within 47%-53%) and minimal lot-to-lot variation is essential. Routinely production's duty cycle sampling test for lot-to-lot or processing variation is recommended. This duty cycle adjustment technique is also suitable for other differential signals such as LVDS and LVPECL.

References

1. Johnson, H. w., and Graham, M., "High-speed digital design", Prentice Hall, 1993.
2. JEDEC standard, "Stub Series Terminated Logic for 2.5V (SSTL_2)", JESD8-9A, (revision of JESD8-9), December 2000.
3. JEDEC Standard No. 44, "Standard for definition of 'CU877 clock driver for registered DDR2 DIMM applications", JC40 Item No.44, Rev # 0.95; second showing: April, 2002; 5/3/2002