

Reference board User Guide for PI7C8152

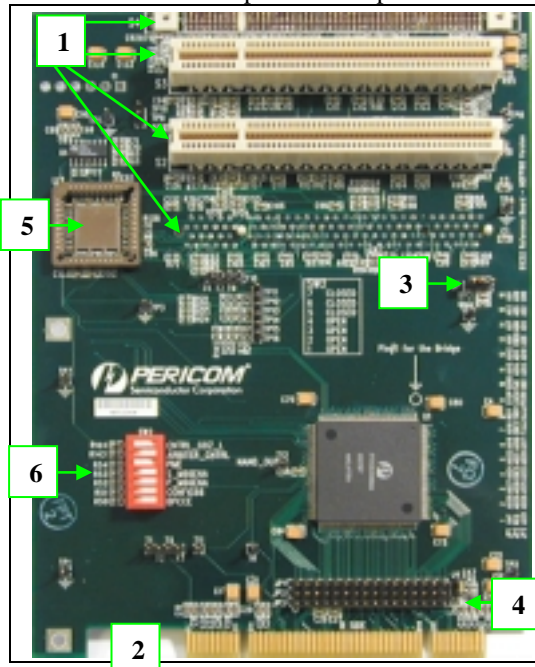
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Introduction

The Pericom PI7C8152 PCI-to-PCI bridge evaluation board demonstrates the bridge and allows testing of key features either before or during design / layout stages. The PI7C8152 PCI Bridge complies with PCI Local Bus specification 2.2, as well as PCI bridge specification 1.1.

Quick start

The numbers on the photo correspond to the text explanation on the right:



- 1) 3 standard, and one straddle mount PCI connectors.
- 2) Pin 1 on the golden PCI edge connector faces left when looking down on the component (bridge IC socket).
- 3) Secondary bus Vio select : 3.3V or 5V
- 4) Headers for sampling signals on the primary PCI bus
- 5) External arbiter socket
- 6) Switch to set speed and misc. functions

This board comes **already configured** to support:

- a) Primary PCI voltage (p_VIO) follows motherboard keying.
- b) Secondary PCI bus voltage is set to **3.3V** at J2
- c) **33 MHz** primary (ie primary bus M66EN is low)
- d) **33 MHz** secondary (ie secondary bus M66EN is low)
- e) **internal arbiter** is enabled
- f) No need to connect external power in most applications; the host PCI bus can power all 4 secondary bus slots.

Default and (*) important switch settings at a glance:
SW1 there is no SW1.

SW2	signal	default	
1	bpcce	On	“off” Enables bus/power clock control function (BPCCE is high)
* 2	cfg66	On	“Off” selects Bridge is 66 MHz capable.
3	p_M66en	On	Reference board can be used in <i>either</i> 66 or 33 MHz motherboard slot.
4	s_M66en	On	“Off” sets Secondary bus is 66 MHz capable (S_M66EN is high)
* 5	PME#	Off	PME# is de-asserted in the off position
* 6	Arbiter_ctrl	On	“On” Internal arbiter is selected
7	Cntrl_GOZ	Off	“Off” pulls SCAN_TM_L high to disable Full Scan Test Mode

Defaults for Jumpers:

- J1** not connected Normally the reference board draws all power from the motherboard
- J2** jumper 2-3 3.3 V secondary bus VIO
- J3** not used
- J4** jump 1-2 Ties P_VIO from motherboard PCI connector to the P_VIO signal to bridge

BEFORE POWERING THE BOARD

a) **Speed selection:** Using the switch SW2, choose the speed setting for the secondary bus based upon the input primary bus speed:

SW2	33/33	66/33 secondary	66/66	Default
2-2 CONFIG66	On	Not supported	Off	Off
2-3 M66EN pri	On	“	Off	Off
2-4 M66EN sec	On	“	Off	Off

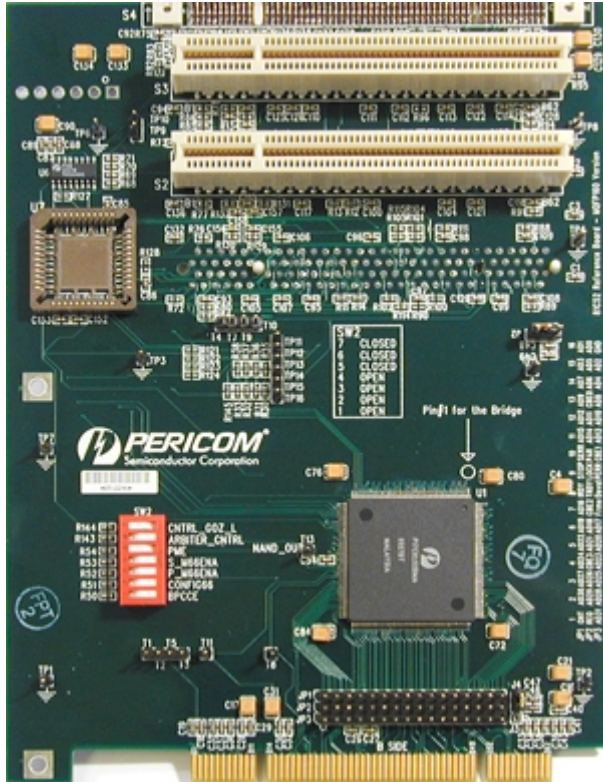
(Note: **The secondary bus will have output clocks at the same frequency of the input primary clock regardless of M66EN status at either bus.**)

b) **Seat the board into a PCI slot on the main system board.** Looking from the front of the motherboard, the small lip on our reference board points to the back of the motherboard and the component side with the PI7C8152 bridge chip is on the left hand side. The motherboard PCI connector is adequate to powering the board with a few add-in cards.

c) **Connect any PCI cards desired on the secondary PCI bus.** For all PCI connectors on our reference board, when looking down onto the bridge IC, pin 1 is on the **left** side of the board. Notice that the external arbiter socket on the top side is closest to PCI connector pin 1. This also applies to the top mounted “straddle” connector. The PCI slots are keyed for 3.3V or universal connector add-in cards; putting in any cards backwards will short 5V to ground through the PCI connector. Also each PCI connector has in white stencil lettering “A1”, “B1”, “A62”, and “B62” at the 4 corners of each slot, as a reminder where pin 1 is on each connector.

At this point, the Pericom PI7C8152 reference board is ready for you to use.

Components and Jumper reference



- U1 Pericom 8152 bridge IC
- U2 not used
- U3 not used
- U4 not used
- U5 not used
- U6 PI3B3257-W Mux/Demux bus switch
- U7 socket for **optional** external arbiter

- SW1 not used
- SW2 speed, options selection
- J1 auxiliary power, **not stuffed**
- J2 secondary bus Vio select
- J3 +3.3V source, **not stuffed**
- J4 primary Vio follows motherboard

TABLE

- a) Right side of board has JP1, JP2, JP3 list
- b) SW2 default stencil list is replaced by this manual.

Switch listing

SW1: (does not exist)

SW2	signal	default	full description
1	bpcce	On	“off” Enables bus/power clock control function (BPCCE is high) “on” puts a low at this signal. (This influences turning off PCI clocks under ACPI power management.)
2	cfg66	On	“Off” selects Bridge is 66 MHz capable . When “On” the bridge is set to 33 MHz on both primary and secondary buses.
3	p_M66en	On	“Off” sets P_M66EN high . Reference board can be used in 66 MHz motherboard slot.
4	s_M66en	On	“Off” sets Secondary bus is 66 MHz capable (S_M66EN is high) “On” forces 33 MHz secondary bus (S_M66EN low)
5	PME#	Off	De-asserts PME# to motherboard, this switch must be “off”
6	Arbctrl	On	“On” selects Internal arbiter ; “off” selects external arbiter <i>but other changes needed also to activate external arbiter</i> . See page 5.
7	Ctrl_GOZ#	Off	Full Scan Test Mode. This switch must be in the “off” position for the board to function.

Jumper block listing

J1 external power connector. left to right [ground, ground, ground, +3.3V, +3.3V, +5V]
Not stuffed, not used. *Pin 1 is +5V, pins 4-6 GND*

J2 Vio select 3-2 **3.3V** (left) 1-2 **5V** (right)

This sets Vio for the secondary bus. The PCI Bridge will drive control signals to this voltage on the secondary bus. This should already be configured for you.

J3 3.3V pin

J3 allows a method to **force** the bridge to use 3.3V signaling for communicating with a 66 MHz motherboard without disturbing the motherboard's Vio, which is only useful when an older motherboard has a 66 MHz PCI bus keyed for 5V. *(This signal is NOT bused into the motherboard Vio.)* **Not stuffed**.

J4 P_Vio select

The topmost pin at **J4** is **P_Vio** from the motherboard and the center pin goes to our bridge.

Primary bus test points **JP1, JP2, JP3:**

These allow a logic analyzer or oscilloscope to monitor signals on the path between the 8150 and primary bus.

There are 3 rows of 16 header pins each, labeled JP1, next JP2, next JP3:

	1	2	3	4	5	6	7	8
JP1	GNT	AD30	AD27	AD24	AD22	AD19	AD16	IRDY
JP2	REQ	AD29	AD26	CBE3	AD21	AD18	CBE2	TRDY
JP3	AD31	AD28	AD25	AD23	AD20	AD17	FRAME	Devsel
	9	10	11	12	13	14	15	16
JP1	STOP	SERR	AD15	AD12	AD9	AD7	AD3	AD1
JP2	LOCK	PAR	AD14	AD11	CBE0	AD6	AD5	AD0
JP3	PERR	CBE1	AD13	AD10	AD8	AD4	AD2	Idsel

(A copy of this table is present on the right hand side of the component side of the reference board.)

Note: correction, JP3-16 should be "IDSEL" not "Ground"

Test points description: These allow convenient sampling of signals by logic analyzer or oscilloscope:

- | | | |
|-------------------------------|---|--|
| T1 Primary TRST GPIO | TP1 ground | TP11 Gnt to 2 nd slot |
| T2 Primary TCK GPIO | TP2 ground | TP12 Gnt to 1 st (bottom) slot |
| T3 Primary TMS GPIO | TP3 ground | TP13 Req to top(4 th) slot |
| T4 INTA# | TP4 ground | TP14 Req to 3 rd slot |
| T5 Primary TDO GPIO | TP5 ground | TP15 Req to 2 nd slot |
| T6 (not present) | TP6 ground | TP16 Req to 1 st (bottom) slot |
| T7 INTB# | TP7 ground | |
| T8 Primary clock input | TP8 ground | |
| T9 INTC# | TP9 Gnt to top (4 th) slot | |
| T10 INTD# | TP10 Gnt to 3 rd slot | |
| T11 Primary Reset# | | |
| T12 (not present) | | |
| T13 SCAN_EN | | |

OPTIONAL External Arbiter:

For **internal** arbiter, **SW2 -6** is ON (closed). This is the **default**.

For **external arbiter**, a number of changes are made to the board:

Move **SW2-6** to **Off** position.

Remove the **0-Ohm** resistors at **R35, R36, R37, R38** to remove connections from slot REQ#s to PCI bridge. Remove **R2** to disable clock connection to slot 1 (bottom most slot).

Add a rework wire from **R2 pin 2** to **R10 pin 1**. This supplies a clock to the external arbiter.

Stuff 0-Ohm resistors into **R121, R122, R123** to add REQ# connections from the external arbiter to each slot. Also, stuff **0-Ohm** resistors at **R127, R128** to add GNT0# and REQ0# connections to the PCI bridge from the External arbiter.

Finally, stuff socket **U5** with an appropriately programmed **Xilinx XC9572 CPLD**
(availability of code TBD)

*The **BOTTOM** slot (connector closest to PCI bridge) is **not** useable in external arbiter mode.*

Asynchronous clock mode: This layout reference board does not have the external clock buffer and oscillator needed for asynchronous secondary bus clock mode.

Where to find more information:

Schematics, bill of materials, gerber files, and technical assistance are all available upon request. Or visit the company website: <http://www.pericom.com/pci/psempart.php?productID=PI7C8152>