WLED Backlighting Solution for Medium-sized LED Panel Designed with AP3064

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1. Introduction

With the enhancement of environment-protection consciousness, WLED backlighting is becoming more and more popular than traditional CCFL backlighting. Nowadays, WLED becomes the mainstream of the small-sized LCD panel backlighting instead of CCFL. Because of so many advantages of WLED, such as fast response, safety, long lifetime, small size and so on, WLED will become more and more important in the medium-sized and large-sized LCD panel backlighting in the future. Compared with the small-sized LCD panel, medium and large-sized LCD panel need tens of WLEDs. It means many new requirements are needed to be met, for example, higher driver voltage and current matching between WLED strings.

BCD semiconductor proposes a WLED backlight solution for medium-sized LCD panel under this condition.

1.1 Solution Description

The BCD solution schematic is shown in Figure 1, which is for 4-channel application, and is designed to drive a total of 72 WLEDs, and the current matching accuracy between any two strings is within ±1.5% .The operation frequency can be adjustable, which allows trade-offs between external component size and system efficiency. WLED brightness can be adjusted by PWM dimming function. The internal soft start circuit effectively reduces the inrush current when starting up. The solution has multiple features to protect the system from fault conditions. It features under voltage lockout protection, over voltage protection, over temperature protection, LED short circuit protection, WLED opens protection and Diode/Inductor short protection.

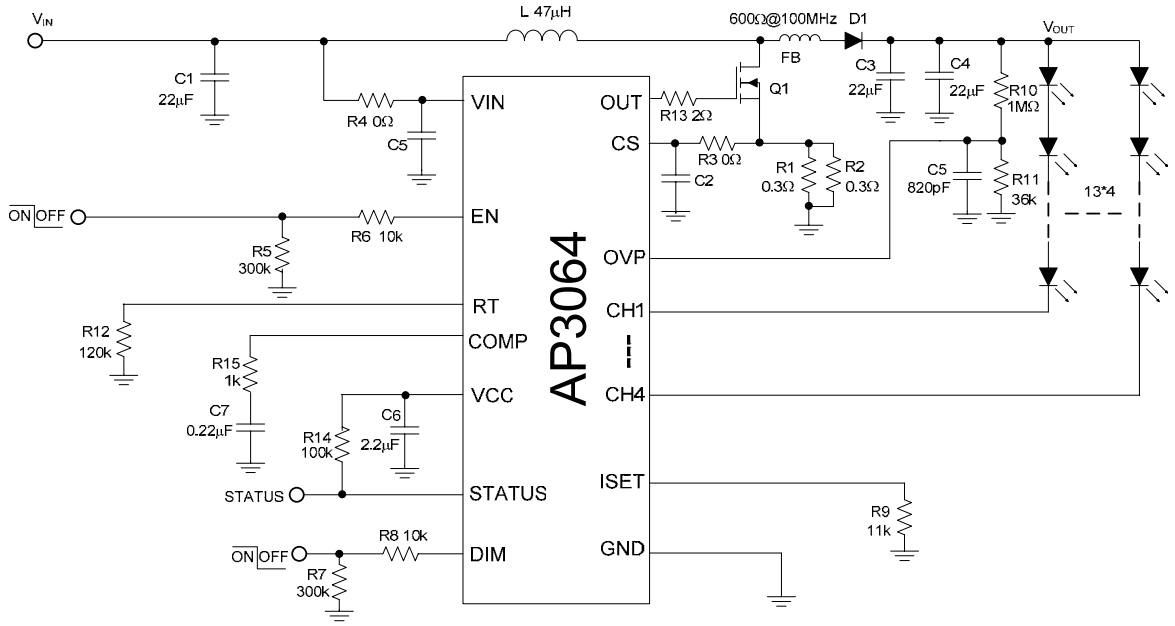

Figure 1. BCD Solution Schematic

1.2 AP3064 Description

The AP3064 is a white LED driver with current balancing and dimming functions. It consists of a boost controller and 4-channel current sinks to drive WLED arrays with constant current from a wide range supply. The full-scale LED current can be adjusted from 20mA to 220mA simply through a resistor. It supports direct PWM dimming. The functional block diagram of AP3064 is shown in Figure 2. The operating process of AP3064 is as follows: at the start of each oscillation cycle, the SR latch is set and the external power switch Q (Refer to Figure 1) turns on with the switch current increasing linearly. The voltage on external sense resistor R_{CS} (Refer to Figure 1) is proportional to the switch current, and is added to a stabilizing ramp, then the result is fed into the non-inversion input of the PWM comparator. When this non-inversion input voltage exceeds inversion input voltage of PWM comparator, which is the output voltage level of the error amplifier (EA), the SR latch is reset and the external power switch turns off. This output voltage level of EA is the amplified signal of the voltage difference between feedback voltage and the reference voltage, the reference voltage is proportional to the LED switch current. It is clear that the voltage level at inversion input of PWM comparator is used to set the peak current level to keep the output in regulation.

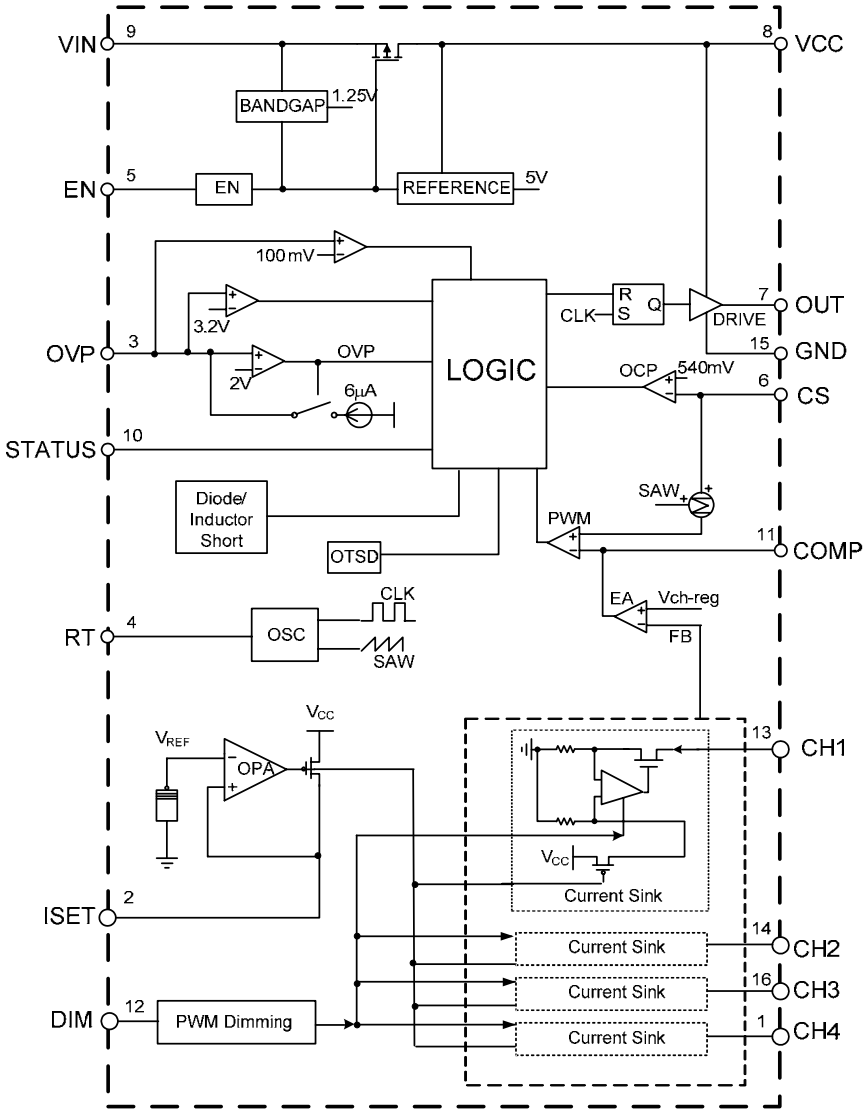

Figure 2. Functional Block Diagram of AP3064

2. Component Selection

In the solution shown in Figure 1, several peripheral components are needed. This section will give some suggestion on how to select these components.

2.1 C_{IN1} Selection

The input capacitor (C_{IN1}) of AP3064 filters the current peaks drawn from the input supply and reduces noise injection into the IC. A 22μF electrolytic capacitor is recommended in the typical application.

2.2 Inductor L Selection

When choosing an inductor, the first step is to determine the operating mode: Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). When CCM mode is chosen, the ripple current and the peak current of the inductor can be minimized. If a small size inductor is required, DCM mode can be chosen. In DCM mode, the inductor ripple current and peak current are higher than those in CCM.

When the value of inductor is less than L_{CCM}(MIN), the system operates in DCM mode.

$$L_{CCM(MIN)} = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \left(\frac{V_{OUT}-V_{IN}}{I_{OUT} * f_{OSC}}\right) * \frac{\eta}{2}$$

Where η is the expected efficiency (the value can be taken from an appropriate curve in the datasheet).

Another important parameter for the inductor is the current rating. After fixing the inductor value, the peak inductor current can be expressed as:

$$I_{PEAK} = I_{IN} + \frac{\Delta i}{2} = \frac{V_{OUT} * I_O}{\eta * V_{IN}} + \frac{(V_{OUT}-V_{IN}) * V_{IN}}{2 * L * f_{OSC} * V_{OUT}}$$

For example, under the typical application of 13S4P (V_{IN}=24V, V_{OUT}(TYP)=42V, V_{OUT}(OVP)=60V, I_{OUT}=720mA, f_{OSC}=430kHz, η=91%), the calculator results are L_{CCM}(MIN)=8.5μH, I_{PEAK}(MIN)=3.96A, considering the I_{PEAK} is too high, finally we choose typical inductor value of 47μH, the calculating I_{PEAK}(TYP)=1.63A, I_{PEAK}(MAX)=2.33A, then we choose the 3A saturation current of the inductor.

2.3 Diode D Selection

The boost converter requires a diode to carry the inductor current during the MOSFET off time. Schottky diodes are recommended due to their fast recovery time and low forward voltage. D should be rated to handle the maximum output voltage (plus switching node ringing) and the peak switch current. The conduction loss of diode is calculated by:

$$P_{DIODE} = I_{RMS\_OFF} * V_F$$

$$\left(I_{RMS\_OFF}^{\ 2} = \left[\frac{V_{IN}}{V_{OUT}} * \left(I_{IN}^{\ 2} + \frac{\Delta I_L^{\ 2}}{12} \right) \right] \right)$$

Where V_F is the forward voltage of the Schottky diode.

2.4 MOSFET Q Selection

When selecting the power MOSFET Q, some tradeoffs between cost, size, and efficiency should be made. Losses in the MOSFET can be calculated by:

$$P_{MOS} = P_{CONDUCTION} + P_G + P_{SW}$$

Where $P_{CONDUCTION}$ is conduction loss, P_G is Gate charging loss, and P_{SW} is switching loss.

$$P_{COUDUCTION} = k_{TH} * I_{RMS\_ON}^{\ 2} * R_{DSON}$$

Where K_{TH} is the factor for the increase in on-resistance of MOSFET due to heating. For an approximate analysis, the factor can be ignored and the maximum on-resistance of the MOSFET can be used.

Gate charging loss, P_G, results from the current required to charge and discharge the Gate capacitance of the power MOSFET and is approximated as:

$$P_G = Q_G * V_{CC} * f_{OSC}$$

Where Q_G is the total gate charge of the MOSFET. Power of VCC is applied by VIN and the MOSFET driving current flows through VCC regulator. This loss P_{VCC} is estimated as:

$$P_{VCC} = (V_{IN} - V_{CC}) * Q_G * f_{OSC}$$

So the total gate charging loss is:

$$P_{G\_TOTAL} = P_G + P_{VCC}$$

The total gate charging loss occurs in IC and not in the MOSFET itself actually.

The switching loss, P_{SW}, occurs in transition period as the MOSFET turns on and off. This loss is consisted of turn-on loss and turn-off loss.

$$P_{TURN\_ON}=\frac{1}{6}\left(I_{IN}-\frac{\Delta I_L}{2}\right)*V_{OUT}*t_{RISING}*f_{OSC}$$

$$P_{TURN\_OFF}=\frac{1}{6}\left(I_{IN}+\frac{\Delta I_L}{2}\right)*V_{OUT}*t_{FALLING}*f_{OSC}$$

$$\Delta I_L=\frac{(V_{OUT}-V_{IN})*V_{IN}}{L*f_{OSC}*V_{OUT}}$$

$$P_{SW}=P_{TURN\_ON}+P_{TURN\_OFF}$$

Where t_{RISING} and $t_{FALLING}$ are the rising and falling time of the MOSFET.

The maximum drain-to-source voltage applied across the MOSFET is V_{OUT} plus the ring due to parasitic inductance and capacitance. The maximum drive voltage at the gate of the MOSFET is V_{CC} plus the ring from gate to source. So the voltage rating of the MOSFET selected must withstand the maximum drain-to-source voltage, and withstand the maximum gate-to-source voltage. The MOSFET with V_{DS}=60V and V_{GS}>5V is recommended in typical application.

2.5 C_{OUT} Selection

The output capacitor of the boost converter is used for output filtering and keeping the loop stable. The ESR value is the most important parameter of the C_{OUT}, because it directly affects the system stability and the output ripple voltage.

The total output ripple can be calculated by the following equations:

$$\Delta V_{OUT}=\Delta V_{OUT}(COUT)+\Delta V_{OUT}(ESR)$$

$$\Delta V_{OUT}(COUT)=\frac{I_{OUT}}{C_{OUT}}*\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}*f_{OSC}}\right)$$

$$\Delta V_{OUT(ESR)}=I_{L\_PEAK}*R_{ESR(CO)}$$

$$(I_{L\_PEAK}=\frac{\Delta I_L}{2}+I_{IN})$$

Where ΔV_{OUT}(COUT) is caused by the charging and discharging on the output capacitor, and ΔV_{OUT}(ESR) is caused by the capacitor's equivalent series resistor (ESR).

To get low output ripple, a low ESR capacitor is a good choice. The capacitance of 2*22µF is recommended.

2.6 R_{OV1} & R_{OV2} Selection

The AP3064 has an Over Voltage Protection (OVP) circuit. Two resistors R_{OV1}, R_{OV2} are connected from OV pin to ground and to the output V_{OUT} (refer to Figure 3)

When the loop is open or the output voltage becomes excessive in any case, the voltage on OV pin will exceed 2.0V, as a result, all functions of AP3064 are disabled and the output voltage will fall. The OVP threshold rising edge can be calculated by:

$$V_{OUT}(OVP)=\left(\frac{R_{OV1}}{R_{OV2}}+1\right)*2V$$

The OVP hysteresis is accomplished with an internal 22µA current source and the operation process is the same as UVLO. The OVP hysteresis can be calculated by:

$$V_{OVP\_HYS}=R_{OV1}*6\mu A$$

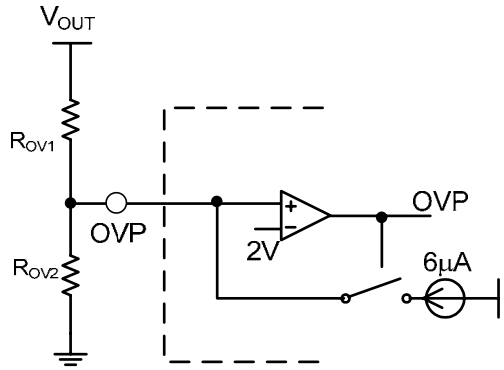

Figure 3. OVP Protection Circuit

2.7 R_T Selection

An external resistor R_T is connected from RT pin to GND to set the operating frequency (refer to Figure 1). The operating frequency ranges from 100kHz to 1MHz. High frequency operation optimizes the regulator for the smallest component size, while low frequency operation can reduce the switch losses.

The approximate operating frequency can be expressed as below:

$$f_{OSC}[MHz]=\frac{52}{R_T[M\Omega]}$$

2.8 R_{ISET} Selection

The WLED current can be set up to 220mA per channel, via the ISET pin. To set the reference current (I_{SET}),

connect a resistor (R_{ISET}) between this pin and ground. The relationship of I_{SET} and R_{ISET} can be expressed by:

$$I_{SET}[mA] = \frac{1200}{R_{ISET}[k\Omega]}$$

The WLED current can be reduced from 100% by PWM dimming control. When≥220mA current is needed in application, two or more channels can be paralleled to provide larger drive current.

2.9 R_{CS} Selection

An external resistor R_{CS} is connected from CS pin to GND to detect switch current signal for current-mode boost converter. The current limit threshold voltage V_{CS} of the AP3064 is fixed at 540mV. The required resistor R_{CS} is dependent on the peak inductor current at the end of the switch on-time, and can be calculated by the following equations:

$$R_{CS\_MAX} < \frac{V_{CS}}{I_{L\_PEAK}}$$

$$P_{RCS} = I_{RMS\_ON}^2 * R_{CS}$$

$$(I_{RMS\_ON}^2 = \frac{V_{OUT} - V_{IN}}{V_{OUT}} * \left(I_{IN}^2 + \frac{\Delta I_L^2}{12} \right))$$

To set the I_{LIMIT}, the resistance of 2*300mΩ is recommended.

2.10 R_C&C_C Selection

The AP3064 integrates the soft start and control loop compensation in COMP Pin. The soft start feature allows the boost converter output to gradually reach the initial steady state output voltage, thereby reducing startup stresses and current surges. The startup time is controlled by an internal 13μA current source and the external compensation capacitor CC which cooperated with R_C to ensure the system have enough bandwidth and phase margin. When powering on, after the V_{IN} UVLO threshold is satisfied, the internal 13μA current source charges the external capacitor C_C. The COMP pin voltage will ramp up slowly and limit the inrush current during startup. C_C=0.22μF is recommended in this system.

The AP3064 adopts current mode PWM control to improve transient response and achieve simple loop compensation circuit. The designer should select R_C and C_C by trial and error, find the appropriate value to ensure the system have enough bandwidth and phase margin. R_C=1kΩ and C_C=0.22μF are sufficient for AP3064 working in 500kHz.

2.11 C_V Selection

The AP3064 includes an internal low dropout linear regulator with the output pin VCC. This pin is used to power internal PWM controller, control logic and MOSFET driver. On the condition that V_{IN}≥5.5V, the regulator generates a 5V supply. If 4.0V<V_{IN}<5.5V, the V_{CC} is equal to V_{IN} minus drop voltage across bypass switch. When V_{IN} is less than 5.5V, connect VCC to VIN.

The VCC pin of AP3064 should be decoupled with a ceramic capacitor placed as close to the pin as possible. This capacitor keeps V_{CC} voltage steady when the system operates at a high frequency. The X5R or X7R ceramic capacitor should be adopted as decoupling capacitor because of their good thermal stability, and the capacitance of 2.2μF is recommended.

3. Operation

3.1 Initialization

When peripheral components are ready, the solution should be initialized by following the below steps.

3.1.1 Power Supply

Add 24V DC voltage to VIN and GND pin to supply the AP3064.

3.1.2 Lighting the 1-to-4 Channels LED

1) Enable the IC: Add 5V DC voltage to EN and GND pin to enable the circuit.

2) Add LED anode to the VOUT pin and add LED cathode to the channel pins. Work with ISET pin resistor to define the channel current. Leave the pin open directly if not used.

3.2 Dimming

After finishing the initialization, the system goes into normal work mode, at this time, the PWM dimming function provides less WLED color distortion and can be used to adjust the LED brightness according to different application. The PWM pin of AP3064 is used to achieve PWM dimming function. The WLED current can be adjusted by applying the PWM signal to PWM pin. At this mode, all enabled channels can be adjusted at the same time and the brightness can be adjusted from 1%×I_{CHX_MAX} to 100%×I_{CHX_MAX}. During the "high level" time of the PWM signal, the WLED turns on and 100% current flows through WLED. During the "low level" time of the PWM signal, the WLED turns off and almost no current flows through WLED, thus changing the average current through WLED and adjusting the LED brightness. The external PWM signal applied to PWM pin should ranges from 100Hz to 20 kHz for good dimming accuracy.

An example for PWM dimming is shown in Figure 4. All 4 channels are set to the maximum current I_{CHX_MAX} at the beginning. When a 50% duty cycle PWM signal is applied to DIM pin, average current valued 50%*I_{CHX_MAX} flows through the 4 channels. When an 80% duty cycle PWM signal is applied to DIM pin, average current valued 80%*I_{CHX_MAX} flows through the 4 channels.

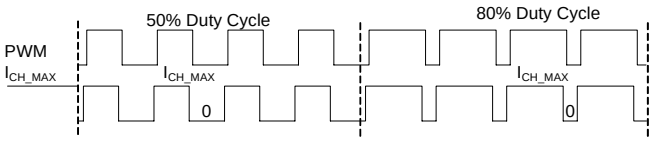

Figure 4. PWM Dimming Mode Example

3.3 Protection

3.3.1 UVLO Protection

The AP3064 provides an under voltage lockout circuit to prevent it from undefined status when startup. The UVLO circuit shuts down the device when VCC drops below 3.8V. The UVLO circuit has 200mV hysteresis, which means the device starts up again when V_{CC} rise to 4.0V.

3.3.2 Over Voltage Protection

The solution has the OV protection. Set the proper OV threshold according to the number of WLEDs in the different applications. The detailed information please refer to 2.6 section. In normal work mode, if any channel is open or excessive output voltage was added, the output will go high. Once the output voltage reaches the OV protection threshold 2.0V, the AP3064 will turn off the external MOSFET and the system goes into hiccup mode and start the LED Open protection The AP3064 will start to work after the output voltage drops below the OV protection threshold and the system goes into enabled mode again.

3.3.3 Open WLED Protection

The solution has the self-check and protection against open WLED. If any used WLED string opens, voltage on the corresponding CHX pin goes to zero and the FB pin of AP3064 exports the zero voltage, V_{OUT} will boost up until the voltage at OVP pin reaches an approximate 2.0V threshold. The IC will automatically ignore the open string(s) whose CHX pin voltage is less than 100mV and the remaining string(s) will continue operation. Once the circuit returns normal operation, the voltage on the CHX pin is regulated to the normal level.

An example is shown in Figure5. If CH4 opens for any reason, the voltage on CH4 goes to zero. FB of AP3064 samples the lowest voltage of CH1, CH2 and CH3, so FB pin exports the zero voltage to make the output voltage go high. As a result, the voltage at AP3064 OVP pin reaches an approximate 2.0V threshold, the AP3064 begins looking for the open channel. After finding the open channel CH4, the AP3064 removes the CH4 from boost control loop, and boost converter returns to normal operation. Once the system returns normal operation, the voltage on the CH1-CH3 are regulated to the normal level.

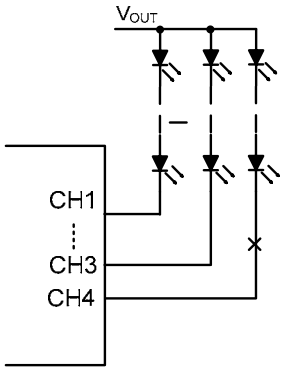

Figure 5. AP3064 WLED Open Protection

3.3.4 Short WLED Protection

The system can avoid destroy when some WLEDs are short. CH1 pin to CH4 pin of AP3064 can endure at least 65V high voltage. During normal operation, any short-circuited LED will cause the corresponding LED pin voltage to rise. If any LED pin voltage exceeds a threshold of approximately 7.3V during normal operation, the corresponding LED current sink will be latched off.

An example is shown in Figure 6, even though the WLEDs of CH3 are all short for any reason, the CH3 LED pin voltage rise to V_{OUT} immediately and exceeds a threshold of approximately 7.3V, the corresponding CH3 LED current sink will be latched off. The AP3064 can still keep the safety.

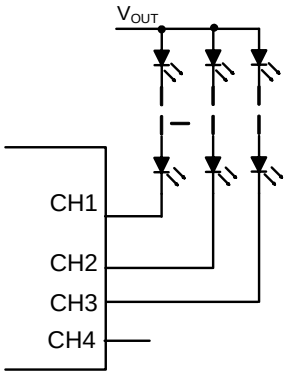

Figure 6. AP3064 WLED Short/Open Protection

3.3.5 Over Temperature Protection
The solution has Over Temperature Protection (OTP). The threshold of the OTP is typically 160ºC, and the hysteresis of the OTP is typically 20 ºC.

3.3.6 Schottky Diode/Inductor1Short Circuit Protection
The AP3064 features Schottky diode/inductor short-circuit protection circuit. When CS pin voltage exceeds 0.8V for greater than 16 switching clocks, the IC will be latched. The voltage of CS is monitored after a short delay of LEB.

3.3.7 VOUT Short /Open Schottky Diode Protection
The AP3064 monitors the OVP pin, if the OVP pin voltage is less than 0.1V, MOSFET drive output will turn off. This protects the converter if the output Schottky diode is open or VOUT is shorted to ground when system startup.

3.3.8 Shut Down under Abnormal Condition
The AP3064 features shut down protection circuit under abnormal condition. When OVP pin voltage exceeds 3.2V, the IC will latch. Toggle EN to restart the IC. This feature can be used for any other protection to shut down the IC.

4. PCB Layout Guideline

Boost converter performance can be seriously affected by poor PCB layout. To produce an optimal solution for medium LCD backlighting, good layout and design of the PCB are as important as the component selection. The following PCB layout guideline should be considered:

4.1 There are two high-current loops in the solution. One is the high-current input loop, and the other is the high-current output loop. The high-current input loop goes from the positive terminal of the CIN1 to the inductor, to the MOSFET, then to the current-sense resistor, and to the CIN1's negative terminal. The high-current output loop goes from the positive terminal of the CIN1 to the inductor, to the diode, to the positive terminal of the COUT, reconnecting between the COUT and the CIN1's ground terminals. Minimize the area of the two high-current loops to avoid excessive switching noise. The trace connected these two high-current loops must be short and thick.

4.2 Create two ground islands. One is called power ground island (PGND), the other is called analog ground island (AGND). PGND consists of CIN1 and COUT ground connections and negative terminal of the current-sense resistor R_{CS}. Maximizing the width of the PGND traces improves efficiency and reduces output voltage ripple and noise spike. AGND consists of the OV, the ISET and RT resistor ground connections, CV, CSS, CC and CIN2 ground connections, and the device`s exposed backside pad. Connect the AGND and the PGND directly to the exposed backside pad. Make no other connections between these separate ground planes.

4.3 Place the bypass capacitor C_V and C_{IN2} as close to the device as possible. The ground connection of these capacitors should be connected directly to AGND pins with a thick trace.

4.4 Keep the feedback trace away from the switching node, and make sure the feedback trace is short and thick. Place the OV detection-divider resistors as close to the OV pin as possible respectively. The divider's center trace should be kept short. Avoid running the sensing trace near switching node.