PI3EQX6701x
PI3EQX6701x SATA ReDriver Application Note

Introduction
PI3EQX6701x SATA ReDriver™ devices are developed to re-drive one full-lane of SAS/SATA signals up to 6Gbps. The devices' features include high- performance continuous-step output swing/pre-emphasis adjustment.

Packaging: 20-contact TQFN (4x4mm)

Main Applications:
- Server
- Desktop
- Storage/Workstation

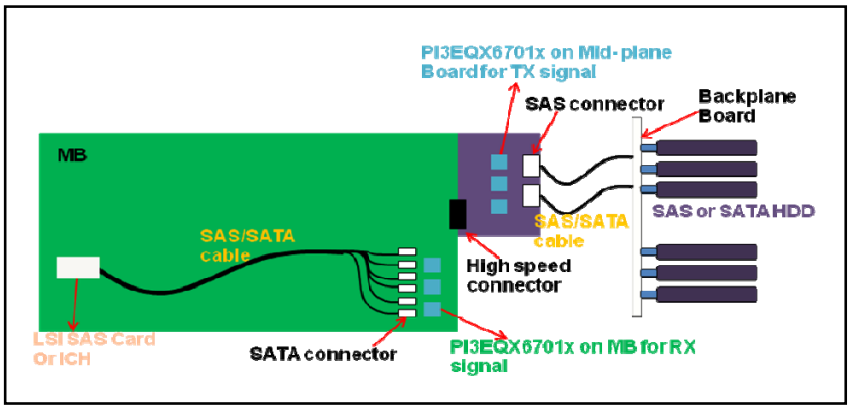


Figure 1a: Example of Typical Application

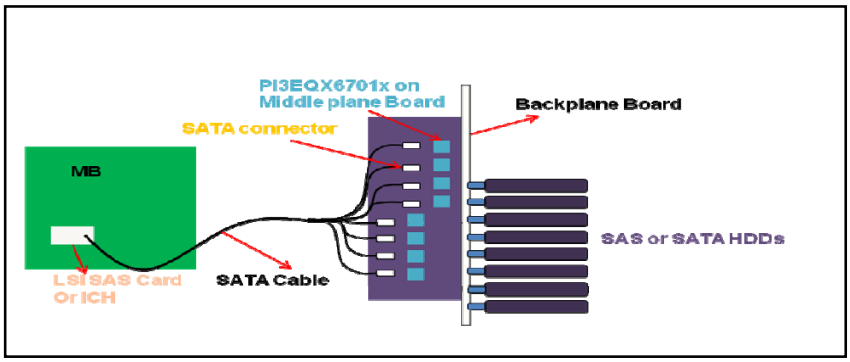


Figure 1b: Example of Typical Application

PI3EQX6701x Part Selection for Various Applications

PI3EQX6701x series devices include PI3EQX6701C, PI3EQX6701D and PI3EQX6701E. These parts' Receiver Equalization characteristics are shown in Table1 below.

		PI3EQX6701C	PI3EQX6701D	PI3EQX6701E
A_EQ	Low	1dB	7dB	1dB
	High	4dB	11dB	4dB
B_EQ	Low	1dB	7dB	7dB
	High	4dB	11dB	11dB
Application Selection		Short trace (<12inch) or cable (<50cm) at input of Channel A&B	Long trace (<30inch) or cable (<1m) at input of Channel A&B	Short trace or cable at input of Channel A Long trace or cable at input of Channel B

Table 1: Receiver Equalization Characteristics

PI3EQX6701x series devices are able to work with 1.2V or 2.5~3.3V power supply. Power consumption of the devices is listed in Table 2 for reference.

Power Supply	Power consumption (mW)	
	Max. (at 900mV Swing, 0db pre-emphasis)	Standby
1.2V Power	244	0.4
2.5~3.3V Power	698	1.1

Table 2: Power consumption at 1.2V and 2.5~3.3V Power Supply

External Components Requirement

PI3EQX6701xZDE series devices require AC coupling capacitors for all redriver inputs and outputs. High-quality, low-ESR, X7R, 10nF, 0402-sized capacitors are recommended.

Layout Design Guide

Layout Considerations for Differential Pairs

- The trace length miss-matching shall be less than 5 mils for the "+" and "–" traces in the same pairs
- Use wider trace width, with 100ohm differential impedance, to minimize the loss for long routes
- Target differential Zo of 100ohm ±20%
- More pair-to-pair spacing for minimal crosstalk coupling, it is recommended to have >3X gap spacing between differential pairs.
- It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces
- The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair.
- Route the differential signals away from other signals and noise sources on the printed circuit board

PCB Layout Trace Routings

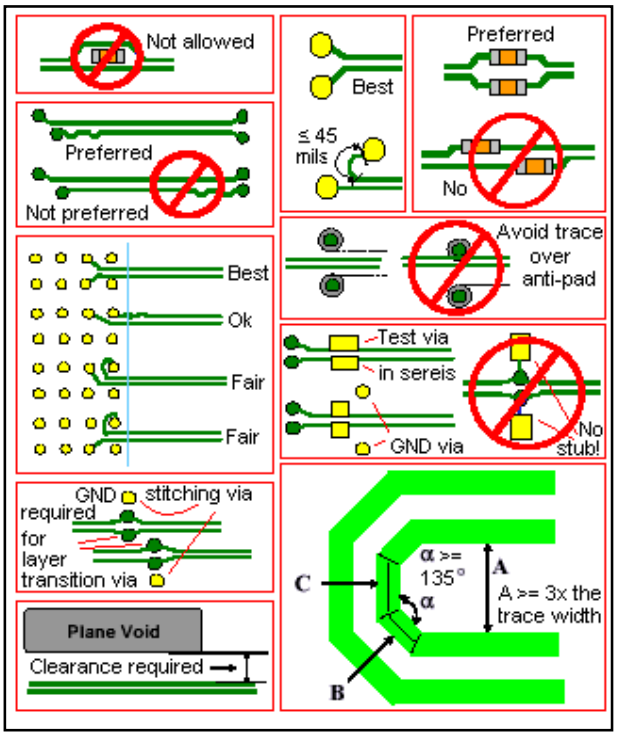


Figure 2: Layout Sample for Trace Routings

Power-Supply Bypass

Designers must pay attention and be careful with the details associated with high-speed design as well as providing a clean power supply; there are some approaches that are recommended.

- The supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The distance to plane should be <50mil.
- The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.
- Careful attention to supply bypassing through the proper use of bypass capacitors is required. A low-ESR 0.01uF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to PI3EQX6701xZDE. Smaller body size capacitors can help facilitate proper component placement.
- The distance of capacitors to IC body should be <100mil.
- One capacitor with capacitance in the range of 1uF to 10uF should be incorporated in the power supply bypassing design as well. It is can be either tantalum or an ultra-low ESR ceramic.

Power Supply Sequencing

Proper power supply sequencing is recommended for all devices. Always apply GND and VDD before applying signals. especially if the signal is not current limited.

Caution: Do NOT exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Equalization Setting

Various Input Traces and Eye Tests with different EQ settings

Figure 3 shows the test setup for testing PI3EQX6701xZDE in different EQ setting. “R” in the figure represents PI3EQX6701xZDE.

Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV, Pre-emphasis is 0dB

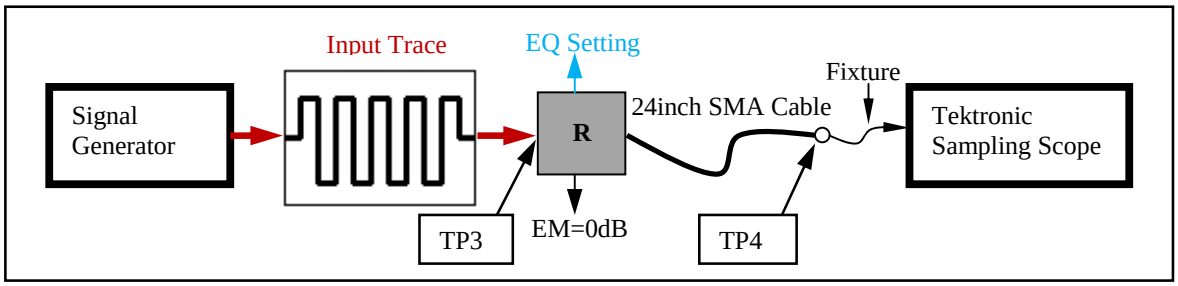


Figure 3: EQ Setting Test Setup for PI3EQX6701xZDE

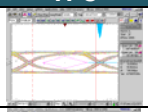
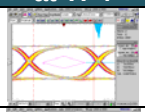
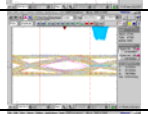
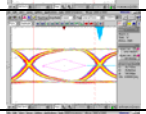
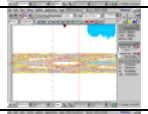
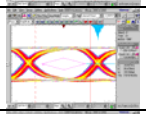
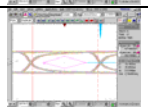
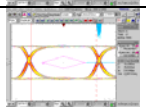
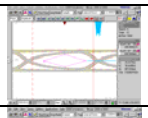
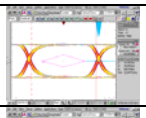
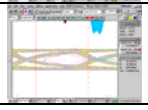
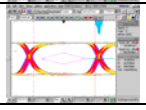
	Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
Eye Diagram vs. EQ setting at 6Gb/s	6 inch FR4 Lab trace (-2dB loss at 3GHz)	1dB (A_EQ or B_EQ =Low)		
	18 inch FR4 Lab trace (-6dB loss at 3GHz)	4dB (A_EQ or B_EQ =Low)		
	30 inch FR4 Lab trace (-10dB at 3GHz)	4dB (A_EQ or B_EQ =Open)		
Eye Diagram vs. EQ setting at 3Gb/s	6 inch FR4 Lab trace (-1.2dB loss at 1.5GHz)	1dB (A_EQ or B_EQ =Low)		
	18 inch FR4 Lab trace (-3dB loss at 1.5GHz)	4dB (A_EQ or B_EQ =Low)		
	30 inch FR4 Lab trace (-5dB loss at 1.5GHz)	4dB (A_EQ or B_EQ =Open)		

Table 3: Eye Diagram vs. Input FR4 trace and EQ Setting at 6Gb/s and 3Gb/s for PI3EQX6701CZDE

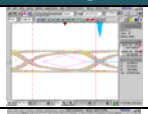
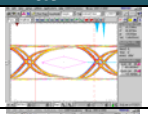
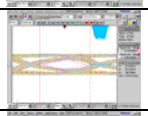
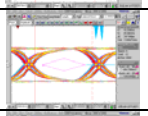
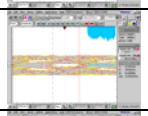
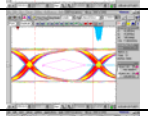
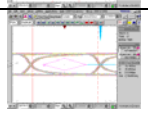
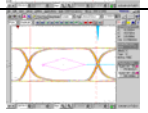
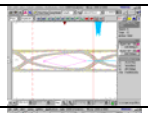
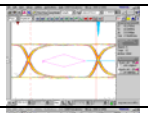
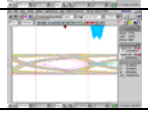
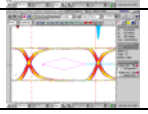
	Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
Eye Diagram vs. EQ setting at 6Gb/s	6 inch FR4 Lab trace (-2dB loss at 3GHz)	7dB (A_EQ or B_EQ =Low)		
	18 inch FR4 Lab trace (-6dB loss at 3GHz)	7dB (A_EQ or B_EQ =Low)		
	30 inch FR4 Lab trace (-10dB at 3GHz)	11dB (A_EQ or B_EQ =Open)		
Eye Diagram vs. EQ setting at 3Gb/s	6 inch FR4 Lab trace (-1.2dB loss at 1.5GHz)	7dB (A_EQ or B_EQ =Low)		
	18 inch FR4 Lab trace (-3dB loss at 1.5GHz)	7dB (A_EQ or B_EQ =Low)		
	30 inch FR4 Lab trace (-5dB loss at 1.5GHz)	7dB (A_EQ or B_EQ =Open)		

Table 4: Eye Diagram vs. Input FR4 trace and EQ Setting at 6Gb/s and 3Gb/s for PI3EQX6701DZDE

PI3EQX6701EZDE uses different EQ settings at A and B channel, but provides the same performance as PI3EQX6701CZDE and PI3EQX6701DZDE.

Output Swing Setting

Figure 4 shows the test setup for testing PI3EQX6701xZDE in different swing settings. “R” in the figure represents PI3EQX6701xZDE.

Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

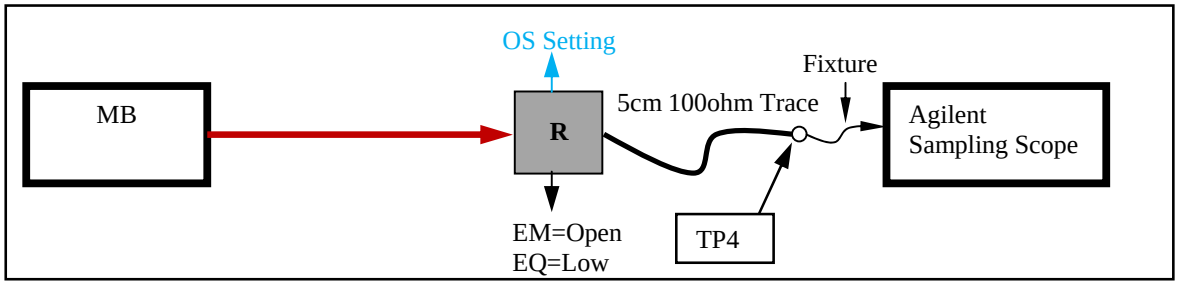


Figure 4: Output Swing Setting Test Setup for PI3EQX6701xZDE

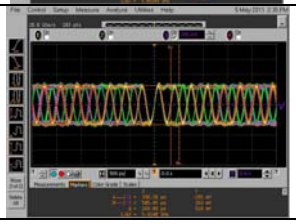
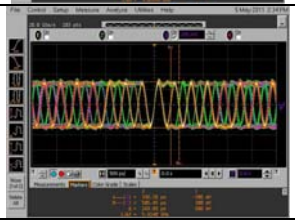
	A/B_OS=2.7kohm	A/B_OS =2.0kohm	A/B_OS =1.0kohm
Output Swing at TP4 vs. OS setting at 3Gb/s			
Output Swing at TP4 vs. OS setting at 6Gb/s			

Table 5: Output Swing vs. Output Swing Setting at 3Gb/s and 6Gb/s for PI3EQX6701xZDE

Pre-emphasis Setting

Figure 5 shows the swing setting test setup for PI3EQX6701xZDE. “R” in the figure represents PI3EQX6701xZDE.

Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

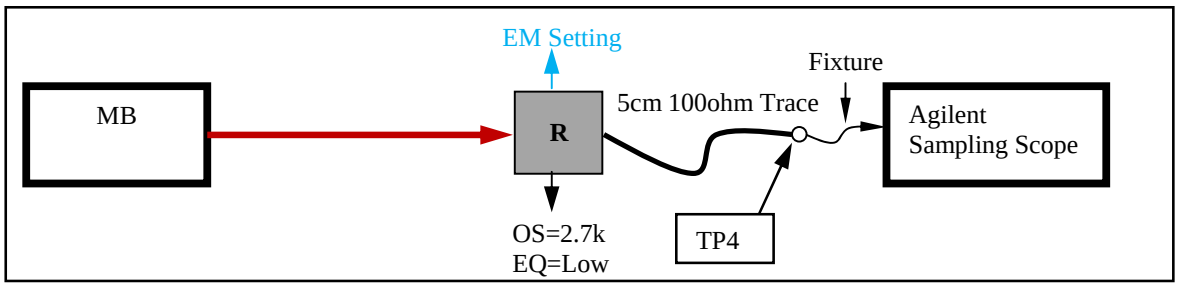


Figure 5: EM Setting Test Setup for PI3EQX6701xZDE

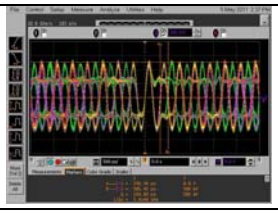
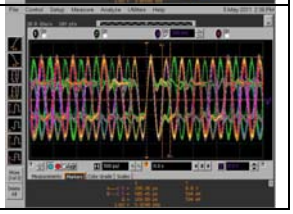
	A/B_ EM=3.0kohm	A/B_ EM =2.0kohm	A/B_ EM =1.0kohm
Output Pre-emphasis at TP4 vs. EM setting at 3Gb/s			
Output Pre-emphasis at TP4 vs. EM setting at 6Gb/s			

Table 5: Pre-emphasis vs. EM Setting at 3Gb/s and 6Gb/s for PI3EQX6701xZDE

Typical Application Circuit

Figure 6a and 6b show typical application circuits of PI3EQX6701xZDE.

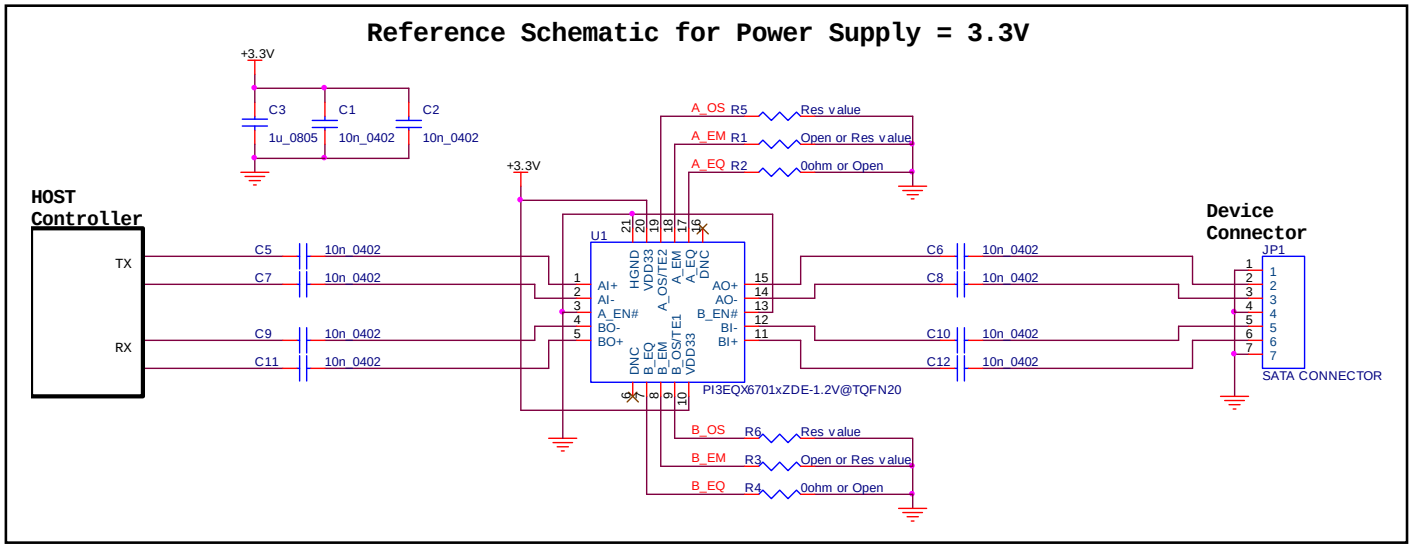


Figure 6a: Typical Application Circuit of PI3EQX6701xZDE using Power=3.3V

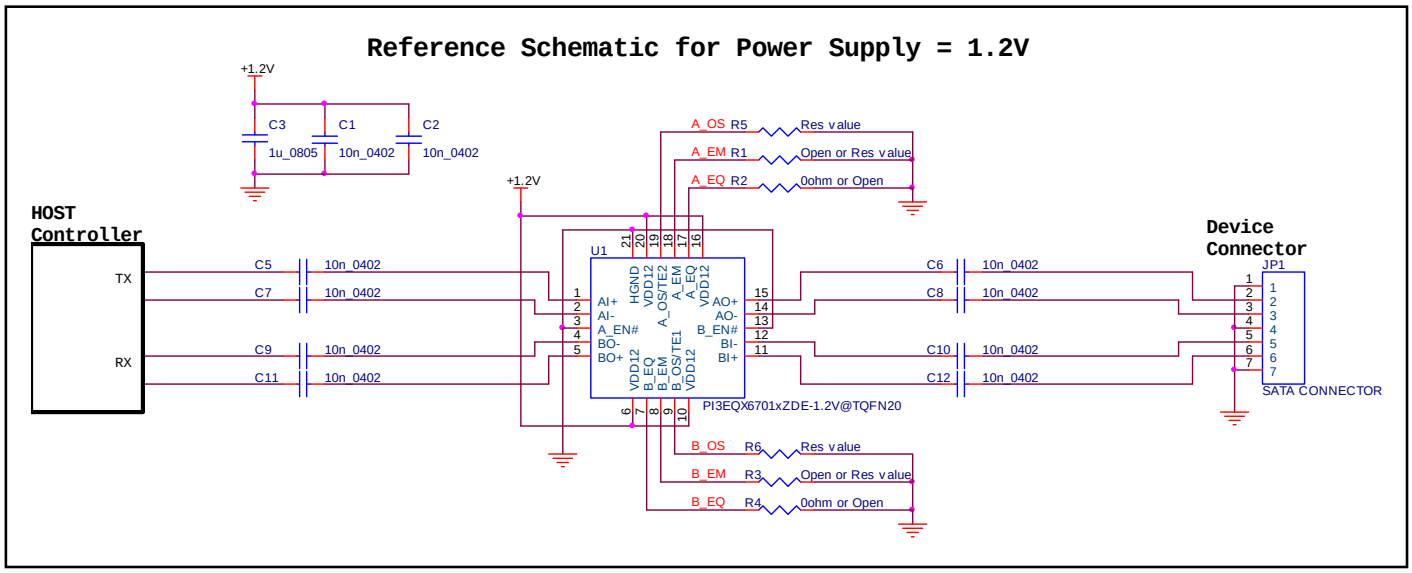


Figure 6b: Typical Application Circuit of PI3EQX6701xZDE using Power=1.2V

Sample PCB Layout

Figure 7a and 7b show typical layout routing of PI3EQX6701xZDE.

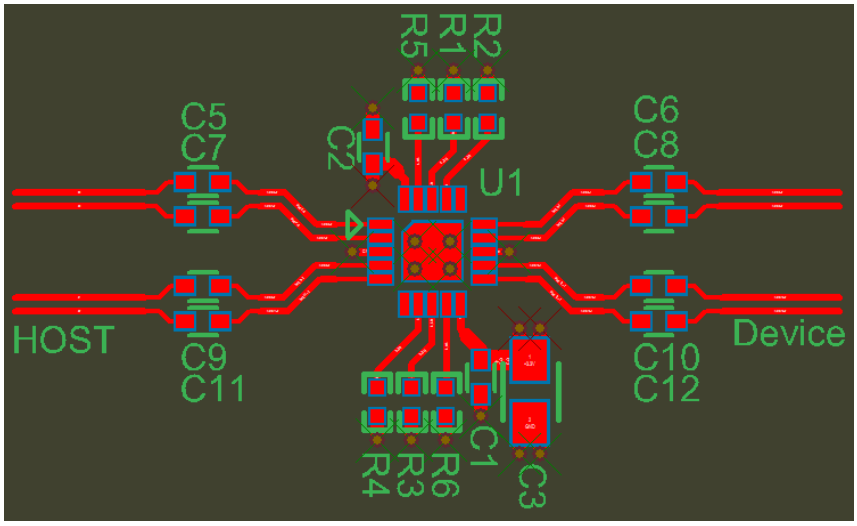


Figure 7a: Typical Layout Routing of PI3EQX6701xZDE using Power=3.3V

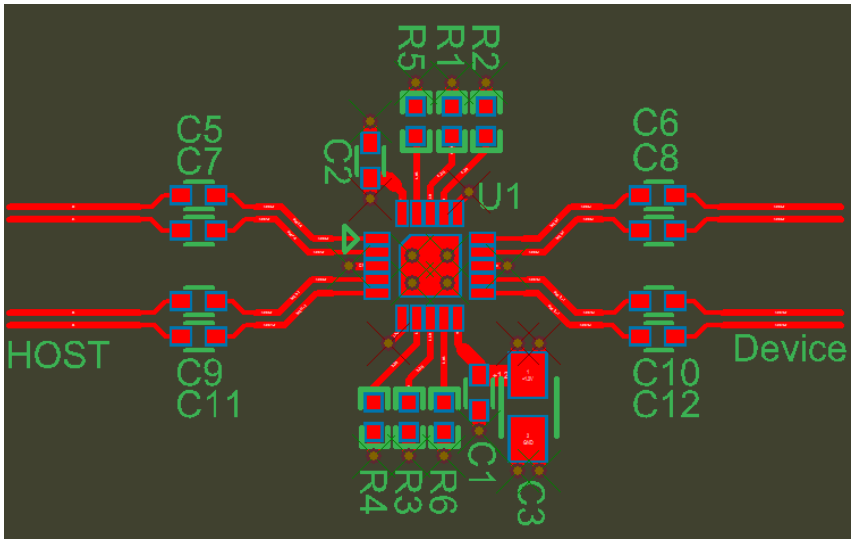


Figure 7b: Typical Layout Routing of PI3EQX6701xZDE using Power=1.2V