PI2DDR3212 and PI3DDR4212
in DDR3/DDR4 applications

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1 Introduction

PI2DDR3212 and PI3DDR4212 are DDR3/DDR4 switches for DDR3/DDR4 and NVDIMM applications.
PI3DDR4212 is designed using 1.8V, 2.5V and 3.3V VDD supply for DDR3/DDR4, POD_12, SSTL_12 and SSTL_15 signaling, with speed up to 5Gbps supporting DDR41600~4266 Mbps transfer rate.
PI2DDR3212 and PI3DDR4212 use Pericom' s proprietary high speed switch technology providing consistent high bandwidth across all channels, with very little insertion loss, cross-talk and bit to bit skew.

2 PI3DDR4212 in NVDIMM application

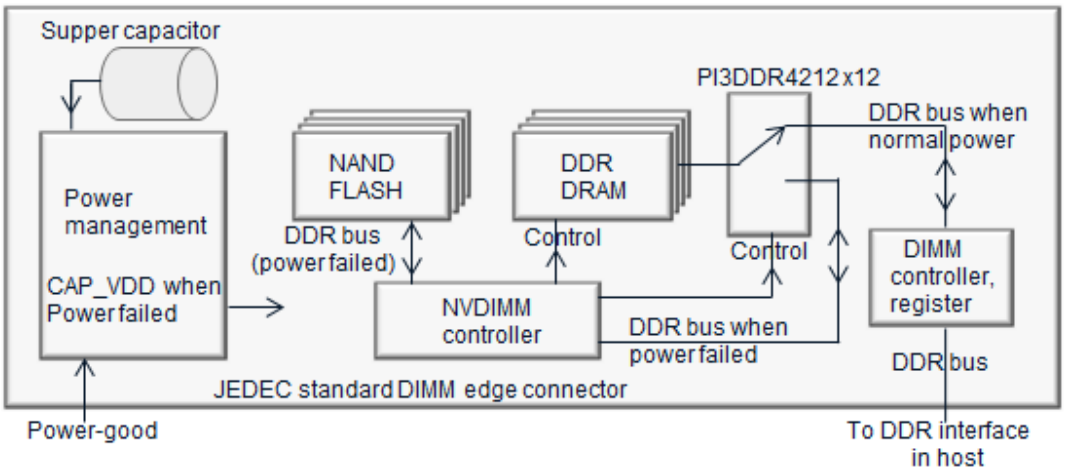

Figure 1: The NVDIMM application using PI3DDR4212

Use PI3DDR4212 in NVDIMM application (figure 1) will provide server systems reliable data backups when system power-failed. The supper capacitor has longer life compared to battery.

- In normal system operation, PI3DDR4212 will route the DDR4 signals between system and the DDR-DRAM for normal data access.
- When system power-failed, the power charged in the supper capacitor will power the NVDIMM-controller to save the data from DDR4-DRAM thru PI3DDR4212 into the non-volatile NAND-FLASH.
- When the system power is back-on, the NVDIMM-controller will re-route the data from the NAND-FLASH thru PI3DDR4212 into the DDR-DRAM to re-start the system normal operation.

3 PI2DDR3212 and PI3DDR4212 in Load Isolation Applications

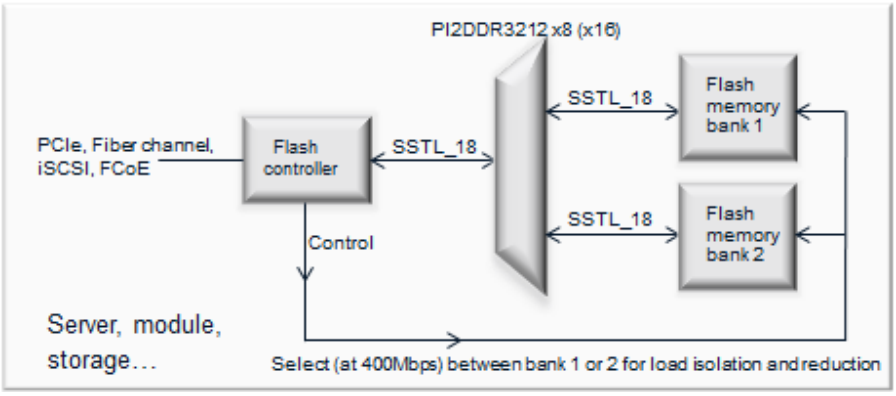

Figure 2: The NVDIMM application using PI3DDR4212

Use PI2DDR3212 and PI3DDR4212 in load isolation application (figure 2) will provide server systems a reliable approach to increase the size of the flash memory without signal integrity problems caused by the double-load from the double memory.

4 Propagation Delay and Compensation

In NVDIMM application, the data signals will go thru PI3DDR4212 with 70ps propagation delay (Tpd). If there were synchronized signals, such as DDR clock signals (or data signals, etc.) not going thru PI3DDR4212, there will be a 70ps time difference in between.

In order to compensate the 70ps timing difference between the DDR clock and data signals, a common approach is to extend 10.64mm (419mil, 70ps) in clock-trace than data-trace. This 10.64mm (70ps) extra length in DDR clock trace will compensate the 70ps propagation delay from PI3DDR4212 to the data signals (figure 2):

- The speed of light is 299,792,458 meters per second, which is 334mm per nanosecond, or 13.15 inch per nanosecond.
- The speed of signals in FR4 trace is about 152.4mm per nanosecond (layout-fabrication dependent), which is about 6 inch per nanosecond, or 0.152mm per picosecond, or 6mil per picosecond.
- All signal switches have propagation delay, such as the 70ps Tpd in PI3DDR4212, which is from the signal travel-time between in-out pins plus the switch RC delay.

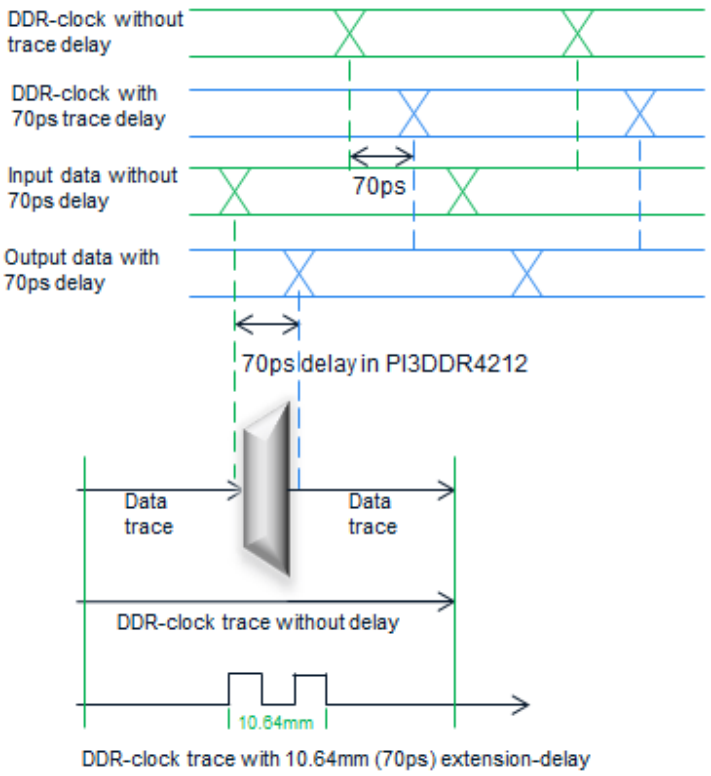

Figure 3: The trace delay compensation to the 70ps propagation delay in PI3DDR4212

5 Insertion loss of PI3DDR4212

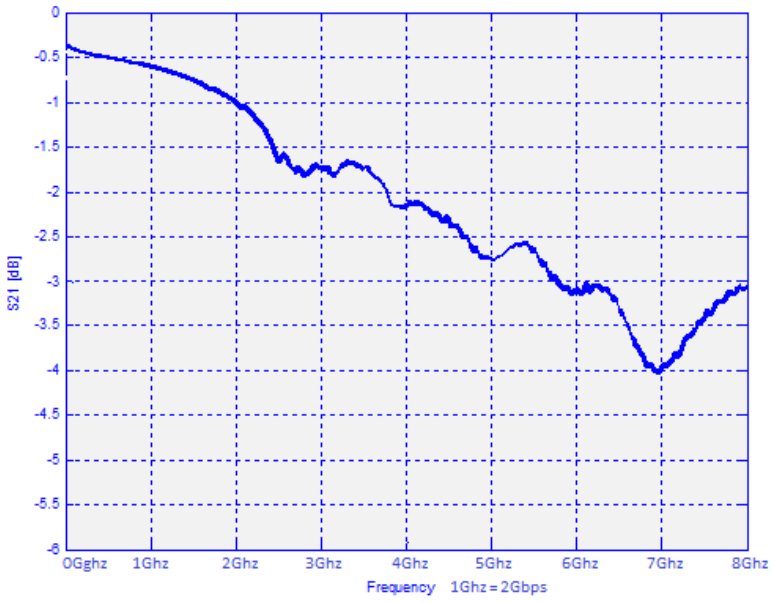

Figure 4: The insertion loss of PI3DDR4212

6 Power and trace

Use 0.1uf bypass capacitors as close to the VDD pins as possible to minimize the power ripper and noise.

Use proper trace impedance according to the DDR3 and DDR4 DIMM standards for impedance matching of each signals.