APPLICATION NOTE 1120
GREEN MODE PWM CONTROLLER

Introduction

The AP3125 series is a low start-up current, current mode PWM controller with green-mode power-saving operation. AP3125 series' PWM switching frequency at normal operation is fixed at 65kHz dithering with a narrow range. The differences between AP3105NX and AP3125 series are shown in Table 1. The dithering of frequency will improve EMI feature. When the load decreases, the frequency will reduce and when at a very low load, the IC will enter "burst mode" to minimize switching loss. A minimum 20kHz frequency switching is to avoid the audible noise as well as reducing the standby loss. A so-called VCC Maintain Mode is applied under light load to realize a stable output and to reduce the loss on the start-up resistor. The standby power of the system using AP3125 series can be less than 75mW at 230V input.

	AP3105NX	AP3125 Series
Frequency	Fixed with 65kHz	Fixed with 65kHz (AP3125A/V/R/L/B/ST) 100kHz (AP3125HA/HB)
VFB Resistor	10kΩ	15kΩ
Standby Performance	Better	Best
External Protection by PIN 3	OTP, OVP	OTP, OVP, SOVP, BNO
Internal OTP	NA	Auto-recoverable
OCP Curve Balanced	Better	Best

Table 1. The Differences between AP3105NX and AP3125 Series

The AP3125 series integrates a lot of functions such as the Lead Edge Blanking (LEB) of the current sensing, internal slope compensation and several protection features which include cycle-by-cycle current limit (OCP), fast OCP (FOCP), VCC over voltage protection, OTP, OLP protection. The AP3125A/V/L/R's "CTRL" pin is designed for customers to add external protection functions such as OVP and OTP while AP3125B is equipped with built-in Brownout (BNO) and Line Over Voltage Protection (LOVP).

The AP3125 series is specially designed for off-line AC-DC power supply, such as LCD monitors, notebook adapter and battery charger applications. It can offer the designers a cost effective solution while keeping versatile protection features. The IC uses SOT26 package type to realize its compact size.

This application note includes detailed explanation of the IC's major functions, some considerations about the PCB layout, and methods for reducing the standby power loss.

Function Description

2.1 CTRL Pin (AP3125A/V/L/R)

For some applications, the system requires external programmable protection function. The AP3125A/V/L/R's CTRL pin has two kinds of modes to trigger the protection: high level trigger and low level trigger. The low threshold voltage is 1V and high threshold is 3V. When the CTRL pin voltage is lower than 1V or higher than 3V, latch or auto-restart protection will be triggered (different sub-versions of AP3125 series offer different protection combination, which is shown in Table 2).

Version	VCC OVP	OLP&FOCP	CTRL (Low)	CTRL (High)
AP3125A	Auto-recoverable	Auto-recoverable	Latch	Auto-recoverable
AP3125V	Latch	Auto-recoverable	Latch	Latch
AP3125L	Latch	Latch	Latch	Latch
AP3125R	Auto-recoverable	Auto-recoverable	Auto-recoverable	Latch

Table 2. Version Classification of AP3125 Series

Function Description (Cont.)

CTRL pin voltage maintains 1.6V if the pin is floating, so leave it open if the designer does not need this function. Once the latch protection is triggered, the bulk capacitor will provide the energy to the IC through start-up resistor to ensure the IC disable the output signal (latch mode). This mode will not be released until the AC input is shut off.

Therefore, the de-latch time is mainly depending on the value of HV startup bulk capacitor. If the system needs a short de-latch time, it is better for the startup resistor to take power from the point before the rectifier bridge. Typical application of CTRL pin is shown in Figure 1.

Notes:

1. The sink current to the CTRL pin should be lower than 5mA by selecting a proper pull-up resistor.
2. If the designer needs to apply a bypass capacitor on CTRL pin, the capacitance should not be higher than 1nF.

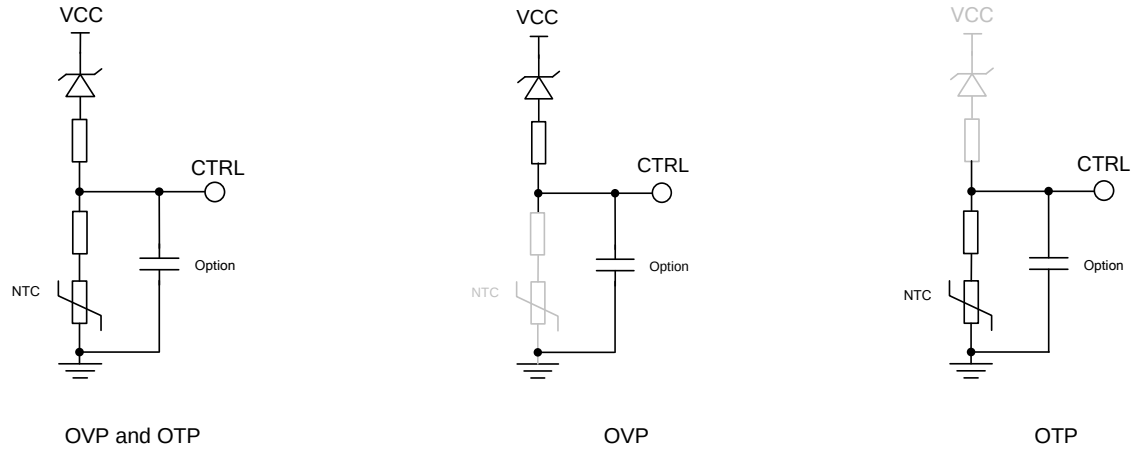

Figure 1. CTRL Pin Application

2.2 BNO Pin (AP3125B/HB)

To avoid potential high current stress at low line voltage, AP3125B/HB introduces reliable brownout protection. AC line voltage information is sampled through a resistor divider net-work (shown in Figure 2), adjusting the divider ratio to achieve expected brownout protection voltage. The resistor divider can connect to either AC line or bulk capacitor. A typical 1nF to 10nF capacitor is strongly recommended to parallel with BNO pin to bypass any accidental spike in AC line for preventing false trigger. When the voltage across BNO pin is higher than 0.95V and VCC reaches UVLO/ON, the GATE pin will output driving signals. If the BNO voltage falls below 0.9V and lasts for 50ms, the GATE pin will turn off and the system will enter hiccup mode until the line voltage rises over its brown-in voltage again.

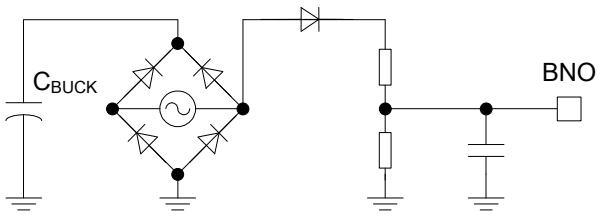

Figure 2. BNO Pin Application

2.3 SOVP/OTP Pin (AP3125ST)

AP3125A/V/L/R can achieve output over voltage protection by pulling CTRL pin high through a Zener diode connecting to VCC. However, this method cannot provide a precise protecting voltage, and a simpler and more precise control method is introduced to AP3125ST with SOVP/OTP pin. The SOVP/OTP pin compares an inner threshold with the divided voltage from the VCC winding, shown as Figure 3 and Figure 4. This divided voltage is sampled after 3μs delay of PWM falling edge as SOVP signal, if the SOVP signal is higher than 3.5V and lasts for 6 to 7 switching cycles,

Function Description (Cont.)

AP3125ST will enter the auto-recovery protection mode. Since the value of VCC winding's waveform reflects the output voltage precisely, the precise output OVP is realized by this function.

Meanwhile, in the duration that switch turning on, SOVP/OTP pin outputs a source current (100μA) to build a voltage on the NTC (in Figure 3) and R2, the IC samples the OTP signal at the falling edge of PWM and compares to the 1V threshold, if this voltage is lower than 1V, AP3125ST enters Latch protection mode as OTP.

D2 in Figure 3 is to clamp the negative signal from VCC winding as a noise immunity solution.

A typical value of low-side resistor is 8k. Since a normal NTC will be 2k around 100~110deg, the total pull-low value will be less than 10k. 1V threshold will be triggered when the temperature increases over +100°C.

To ensure good OTP performance, a NTC with 100KΩ resistance at +25°C is strongly recommended. Otherwise, most NTC has a paralleled parasitic capacitance, this small capacitor will be charged by the 100μA current source during switch turning on and discharge through NTC during switch turning off. At low temperature like -5°C, the NTC resistance will increase to hundreds of KΩ and the discharge time maybe too long to hold a higher voltage on SOVP signal, this abnormal higher voltage will false trigger the SOVP at low temperature. Parallel a resistor R_P to NTC shown as Figure 3 will solve the problem and nearly have no impact on OTP point. Typically the R_P can be 40KΩ for 100KΩ NTC with several pF parasitic capacitance.

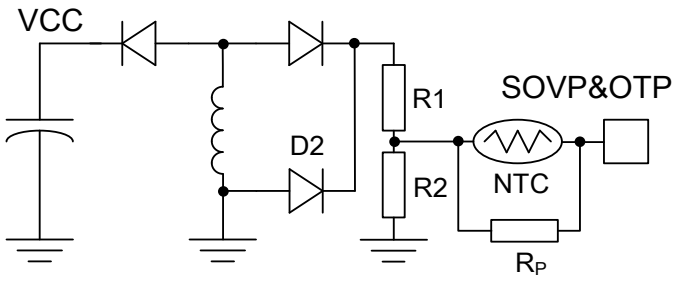

Figure 3. SOVP/OTP Pin Application

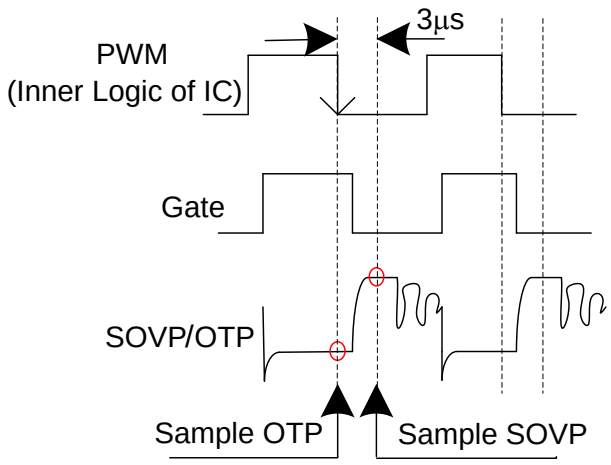

Figure 4. Sample Point of SOVP and OTP

Function Description (Cont.)

2.4 BNO/OTP Pin (AP3125BT)

AP3125BT combines both brownout protection function and external OTP function.

AC line voltage information is sampled through a voltage divider network, adjusting the divider ratio can achieve expected brownout protection voltage. When the voltage across BNO/OTP pin is higher than 0.325V and VCC reaches UVLO/ON, the GATE pin will output drive signals. If the pin 3 voltage falls below 0.3V and lasts for 70ms, the GATE pin will turn off and the system will enter hiccup mode until the line voltage rises over its brown-in voltage again.

When the voltage of BNO/OTP pin is lower than 0.1V, BNO/OTP pin outputs a source current (100μA) to build an OTP detect voltage through D1, D2, NTC and R3 (as in Figure 5), when this voltage is lower than 1.5V, AP3125BT enters Latch protection mode as OTP. This source current (100μA) will only last for 2ms when switching frequency is 65kHz.

Figure 5 shows a typical parameters which set the brown-in point at about 75V and brown-out point at 69V. D1 and D2 are used for blocking current through NTC and R3 when BNO/OTP pin is realizing Brown-in/out function.D1,D2 must be low leakage current and low parasitical capacitor type (like BAS116 of Diodes) to avoid variation of brown in/out voltage under different temperature. The selection of NTC and R3 should follow the formula shown as below:

$$\mathrm{NTC_{OTP}} + \mathrm{R3} = \frac{(1.5\mathrm{V} - 2*\mathrm{V_D})*1000}{100\mu\mathrm{A} - 1000*{}^{1.5V}/_{\mathrm{R2}}}\ \mathrm{K\Omega}$$

Where, $\mathrm{NTC_{OTP}}$ is the remainder resistance of NTC at OTP, $\mathrm{V_D}$ is the forward voltage of D1/D2 at OTP.

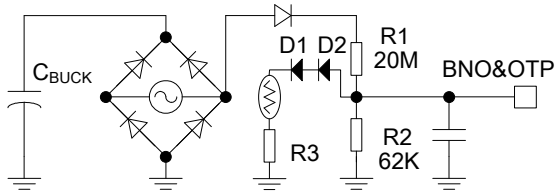

Figure 5. BNO/OTP Pin Application

2.5 Longer OLP Delay Time for Capacitive Load

A capacitive load needs more power to be charged at start-up time. One solution is to enlarge the OCP point and keep the same start-up time, otherwise it will trigger OLP protection mode. Another solution is to extend the OCP delay time, which can simplify the transformer design since there is no need to raise the OCP point. Thus AP3125 series makes the OLP delay time longer to 100ms at start-up and shorter to 70ms at normal operation. If FB pin's value is over 4V for 70ms at normal operation, IC will enter OLP mode to limit the input power. Figure 6 and Figure 7 show the startup process with different OLP delay time under capacitive load. A shorter delay time may trigger OLP under capacitive load while a longer OLP delay time ensures successful start-up.

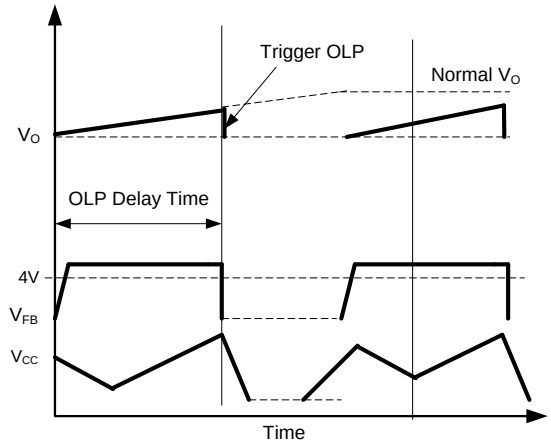

Figure 6. Shorter OLP Delay Time

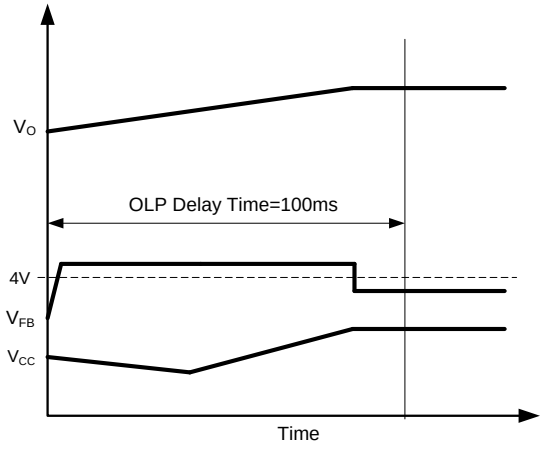

Figure 7. Longer OLP Delay Time

Function Description (Cont.)

2.6 Fast OCP Function

When the load is short-circuited, the power converter can be protected by OLP protection. But if the output filter inductor and the secondary Schottky is short-circuited, the transformer will be immediately saturated resulting in the breakdown of the MOSFET due to high current stress. The AP3125 series bears built-in fast OCP function to alleviate the saturation of the transformer and reduces the current stress of MOSFET. The FOCP position and FOCP waveform are shown in Figure 9 and Figure 10. When the secondary Schottky and the output filter inductor is short-circuited, the power converter can trigger latch or auto-restart immediately within several switching cycles with fast OCP. The FOCP threshold on SENSE pin is 1.7V.

In some applications, high spike voltage appears on the rising edge of the SENSE pin waveform due to a large transformer primary winding's parasitic capacitor or an irrational PCB layout, which may exceed the 1.7V threshold and false trigger FOCP protection (shown as Figure 8). To avoid this result, a RC filter is added on SENSE pin. The recommended resistor value of filter is over 680Ω when the capacitor is 33pF~330pF.

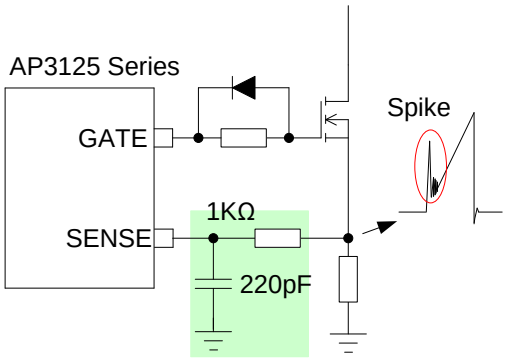

Figure 8. Sense Pin RC Filter

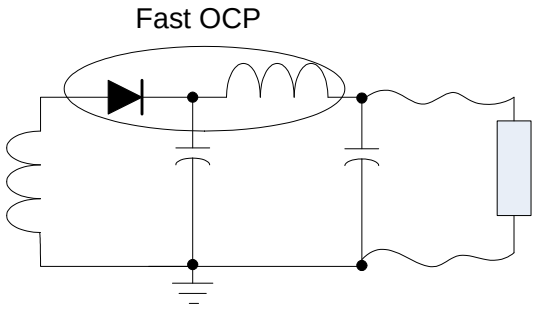

Figure 9. FOCP Position

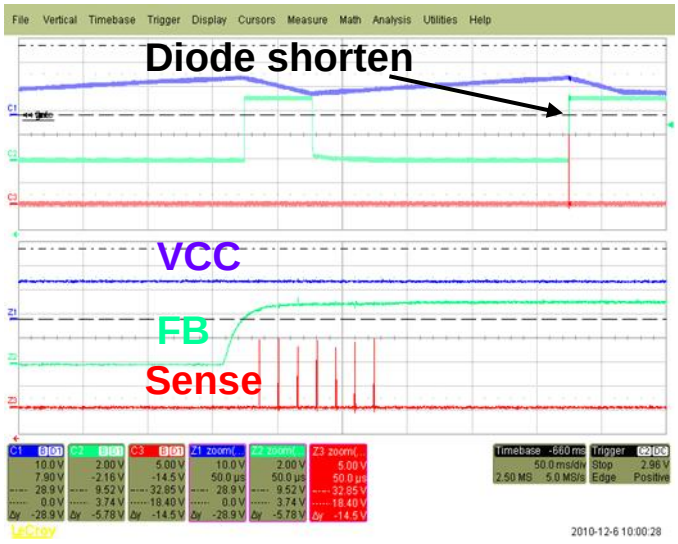

Figure 10. FOCP Waveform

2.7 VCC Maintain Mode

Under ultra light load or load transient condition, V_{FB} will drop to lower than 1.55V, thus the PWM driving signal will be stopped, and there is no more energy transferred due to no switching. Therefore, the IC supply voltage may drop to the UVLO (off) threshold and the system may enter the unexpected restart mode. To avoid this situation, the AP3125 series holds a so-called V_{CC} maintain mode which can supply energy to VCC. When

Function Description (Cont.)

V_{CC} decreases to a setting threshold (9V), the VCC maintain comparator will output a driving signal to make the system switch and provide a proper energy to VCC pin. When V_{CC} increases to 9.5V, the gate signal will be stopped. The VCC maintain function will cooperate with the PWM and the burst mode loop to make the output voltage variation be within the regulation. This mode is designed for reducing startup resistor loss and it will achieve a better standby performance with low value VCC capacitor and larger startup resistor. The V_{CC} will not reduce to the UVLO (off) threshold during the startup process and under ultra light load or load transient condition. To avoid the "VCC maintain mode" triggering in normal operating condition, it is suggested to design the V_{CC} value higher than VCC maintain threshold under minimum load condition. The processing of VCC maintain mode is shown in Figure 11.

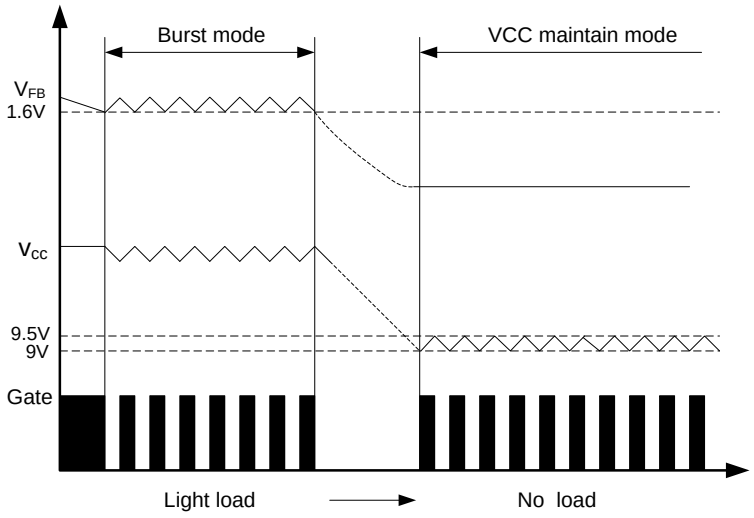

Figure 11. The Process of VCC Maintain Mode

Application Know How

3.1 Surge Immunity Enhanced Solutions

In some applications, a strict surge test specification is required. For instance, common mode surge is over 6kV.

When a large surge voltage is added cross the primary and secondary sides of the system, the general Ground may be raised higher, thus a current will be thrown out from some pins and damage the internal circuit.

If CTRL pin is not floating, R2 is recommended several kilo-ohms for eliminating the abnormal current. Also R1 is suggested to be over 680Ω if it is needed to pass 6kV CM spec.

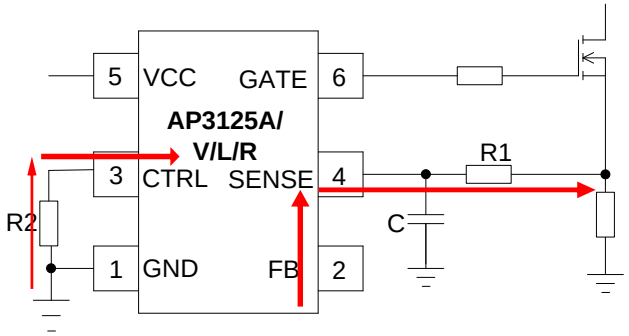

Figure 12. Surge Immunity Circuits

Application Know How (Cont.)

3.2 MOSFET Driver Circuit

A MOSFET consists of many small MOSFET cells. For these cells have different distances from the GATE pin, insufficiency turn on/off speed will cause partial over-heating of the MOSFET and lower efficiency.

For system which is over 36W, driver circuit with a push-pull as shown in Figure 13 (a) is recommended or at least using Figure 13 (b) with a single pull-down transistor. Figure 13 (c) can be applied in system that is less than 36W.

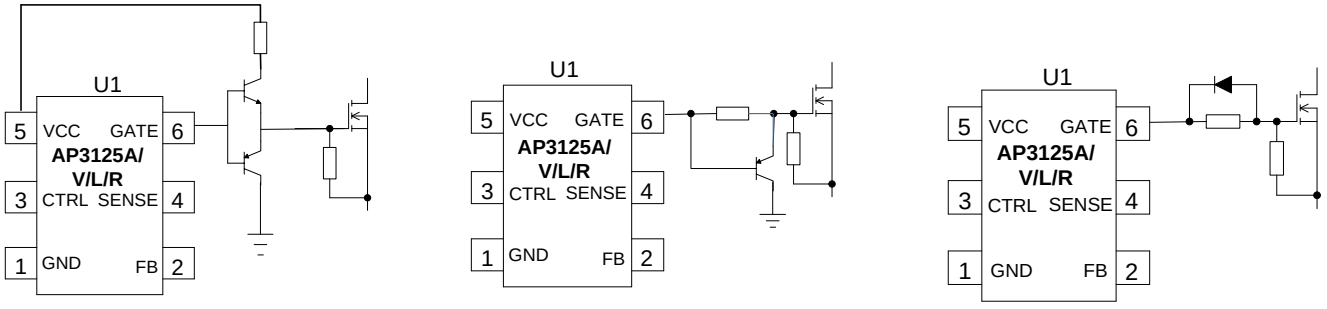

Figure 13. Driver Circuit

3.3 Start-up Circuit

A usual applied start-up circuit takes start-up current from Bus cap (shown as Figure 14 (b)), but the de-latch time of some protection mode when AC turns off will be long for the Bus cap still charges the VCC capacitor.

Another startup circuit (shown as in Figure 14 (a)) is connected ahead of bridge rectifier. It could reset latch mode protection quickly for VCC cap having a single larger discharge current. The de-latch time is equal to:

$$t_{delatch} = \frac{c_{vcc} \times \Delta v}{I_{delatch}} = \frac{c_{vcc} \times 3.3V}{13uA}$$

C_{VCC} is the VCC cap's value, $I_{delatch}$ is the current that the IC consumed under protection mode. Δ_V is the difference of UVLO threshold and de-latch threshold. Thus, a shorter de-latch time needs a smaller VCC cap value.

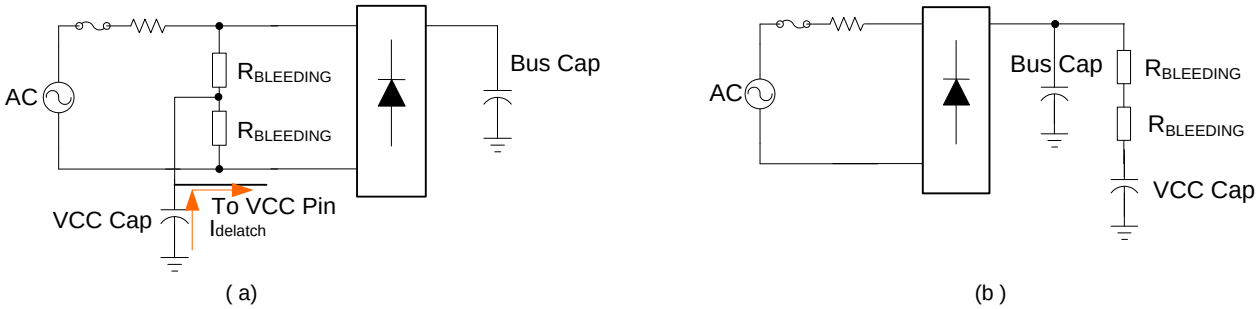

Figure 14. Start-up Circuit

3.4 Standby Power Loss Reduction

Some methods are recommended here for reducing the standby power loss.

X-capacitor and X-resistor

A good quality X-capacitor will be helpful to save the standby power, and a low value X-cap could also decrease the X-cap loss. According to IEC 60950, for the X-cap exceeding 0.1μF, the voltage will be decayed to 37% of its original value during an interval equal to one constant, and after calculating, the RC value is determined by the formula "R×C<1".

Therefore, for a low value X-cap, a higher value X-resistor could be used, and the losses on X-resistor will be reduced.

Application Know How (Cont.)

Current Sampling Resistor

The value of current sampling resistor could affect the standby power. A lower value SENSE resistor is good for low standby power. But it also has an effect on the OLP result; a lower value SENSE resistor will make a larger OLP point.

"SENSE" Pin RC Value

The value of "SENSE" pin RC could also affect the standby power. A larger value of RC can make the I-peak sense signal and the voltage on "FB" pin lower. A lower voltage on "FB" pin will result in a lower operating frequency. It is good for achieving low standby power, but it will also make the OLP point larger.

The Output Voltage Dividing Resistor

The value of output voltage dividing resistor should be as high as possible, but the maximum value of the resistor connected to GND (R17 in Figure 18) should not exceed 15KΩ.

Primary RCD Clamp Circuit

To get a better standby power, the RCD clamp circuit could be replaced by a Transient Voltage Suppressor (TVS) and a diode (Figure 15). The advantage of the TVS clamp is that it only conducts when necessary and it is independent of the switching frequency.

Compared to a RCD clamp, it reduces no-load power but increases costs and EMI. Besides, a lower value of RC is contributed to standby power, while the voltage stress on MOSFET should be in the spec.

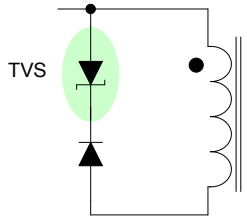

Figure 15. Clamp Circuit with TVS

3.5 SENSE Pin RC Filter Chosen Principle

Table 3 shows the affects with different RC value on SENSE pin. A proper value of R_F is 680Ω to 2.5kΩ while the C_F value is 33pF to 330pF. Figure 16 shows the results of OCP line regulation with different RC value.

	Standby Loss	OCP Line Regulation	FOCP Trigger
Higher RC	less	worse	Not easily
Lower RC	larger	better	More easily

Table 3. Affects of RC value

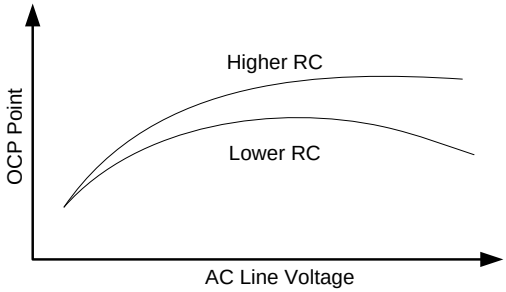

Figure 16. OCP Regulation with Different RC

PCB Layout Consideration

4.1 High Frequency Loop Consideration

As shown in Figure 17, there are four major high frequency current loops:

1. The current path from bulk capacitor, transformer, MOSFET, R_{CS} returning to bulk capacitor
2. The path from GATE pin, MOSFET, R_{CS} returning to the ground of IC
3. The RCD clamp circuit is a high frequency loop
4. Transformer, rectifier diode, and output capacitor is also a high frequency current loop

The loops must be as short as possible to decrease the radiation area for a better EMI, and if the MOSFET and Schottky diode have heat sink, the heat sink should be connected to their ground separately.

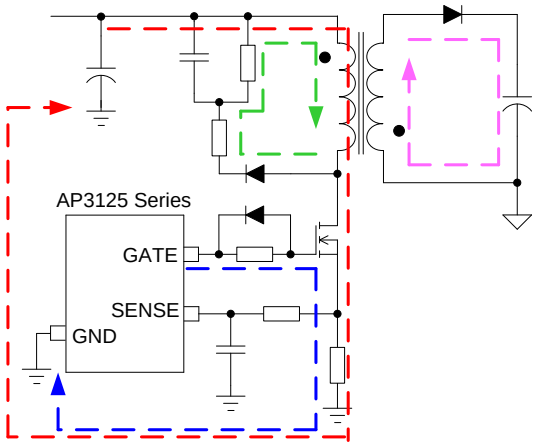

Figure 17. High Current Loop

In addition, the IC should not be placed in the loop of switching power trace, and in some applications, the power ground could be crossed over by the control signal (low current and low voltage), but the switching power trace with pulsating high voltage should not be crossed over.

4.2 ESD Consideration

Electro-Static Discharge (ESD) is an important testing item for switching power supply. The system's ability for bearing the test could be improved by designing a path to release the electric charge to the ground.

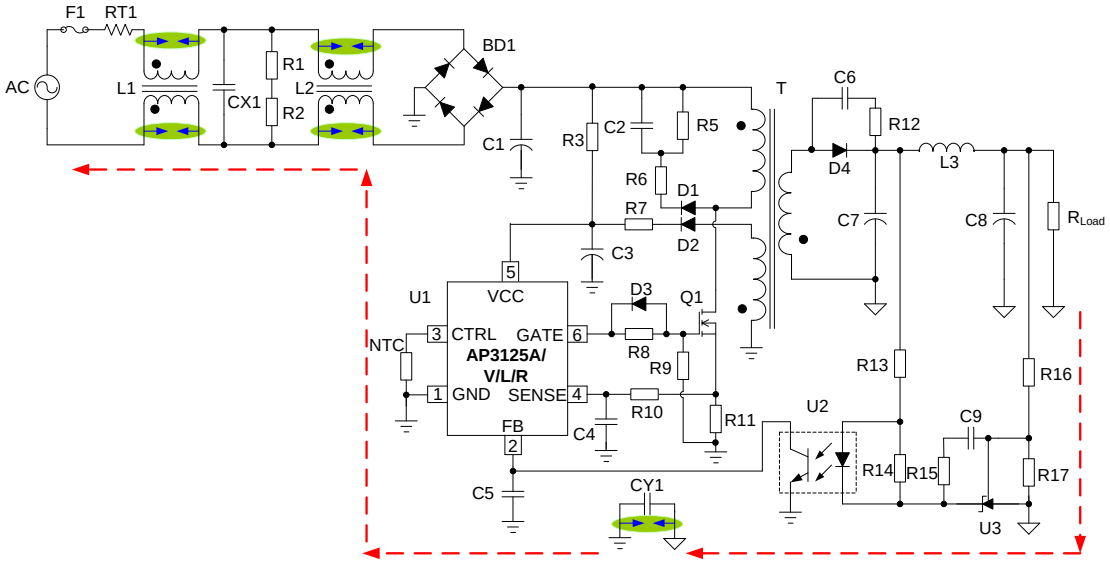

Figure 18. The Path to Release Charge of ESD

PCB Layout Consideration (Cont.)

As shown in Figure 18, the red line represents the proposed path to release the charge. The copper tips for discharging should be placed between primary side and secondary side, but the distance between two copper tips should be consistent with the requirement of the safety specification.

The input common mode filter and differential mode filter will affect the effect of transient discharging, so the copper tips should be added and their distance should be as short as possible. Another way is placing a resistor paralleled with the inductor to replace the copper tip and the resistor's value is about 1kΩ to 5kΩ. A smaller resistor is helpful to ESD but has bad effect on lighting surge.

4.3 Layout Consideration for Surge Test

Figure 19 shows a circuit example which is under lightning surge test. The surge signal is across between input line cable and secondary earth ground. Possible surge current paths, I1, I2 and I3 are shown in the diagram.

I2 is the current which is passing through YCAP, and I3 is the current which passing through transformer from secondary GND to primary Aux winding GND. I2 and I3 may interferes IC GND if YCAP GND and AUX GND has common trace on the layout. I1 is the current which is passing through transformer from secondary GND to primary bulk CAP. I1 normally will not influence IC because there is large resistor between IC pin to bulk CAP terminal.

A proper "Ground" layout is a so-called "Star" connection which is highly recommended for primary GND. As shown in Figure 19, the GND of MOSFET, Auxiliary winding GND, Y-cap GND and control IC GND are separated, and finally connected together on bulk capacitor ground. The width of these grounds should be kept as large as possible.

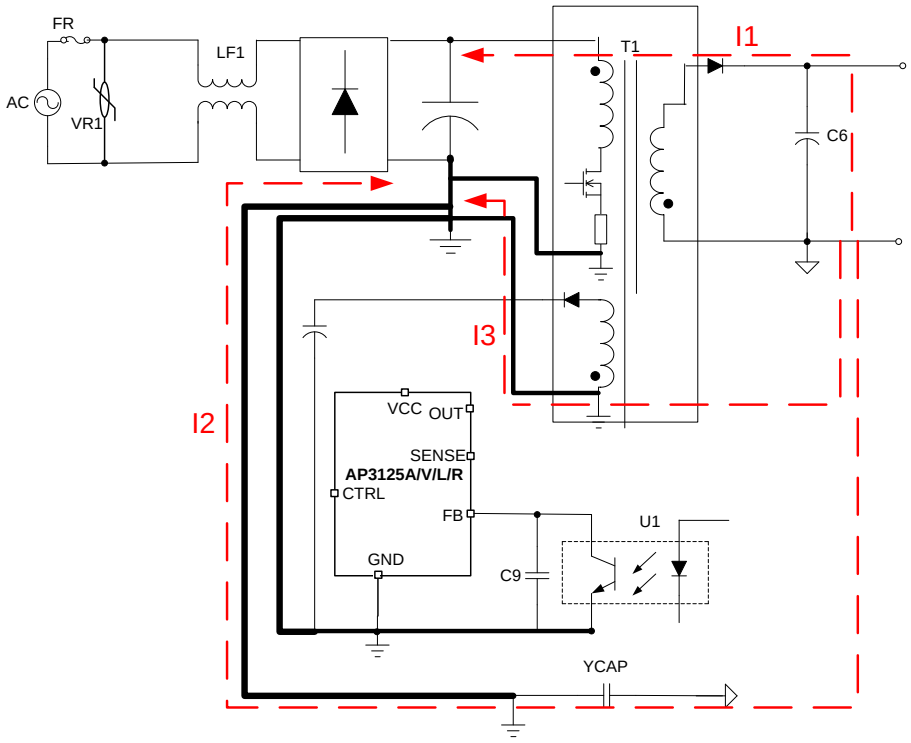

Figure 19. Ground Layout for Surge Test Immunity

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

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