AP3402/20 Application Note

AE Department

1. Revision Information

Date	Revision	Description	Comment
2014/06/12	V1.0	Initial Release	

2. General Description

The AP3402/20 is a 2A step-down DC-DC converter. At heavy load, the constant frequency PWM control performs excellent stability and transient response. No external compensation components are required.

The AP3402/20 supports a range of input voltages from 2.7V to 5.5V, allowing the use of a single Li+/Li- polymer cell, multiple Alkaline/NiMH cell, and other standard power sources. The output voltage is adjustable from 0.6V to the input voltage. The AP3402/20 employs internal power switch and synchronous rectifier to minimize external part count and realize high efficiency. During shutdown, the input is disconnected from the output and the shutdown current is less than 1μA. Other key features include over-temperature and short circuit protection, and under-voltage lockout to prevent deep battery discharge.

The AP3402/20 delivers 2A maximum output current while consuming only 90μA of no-load quiescent current. Ultra-low RDS(ON) integrated MOSFETs and 100% duty cycle operation make the AP3402/20 an ideal choice for high output voltage, high current applications which require a low dropout threshold. The AP3402/20 is available in TSOT26 package.

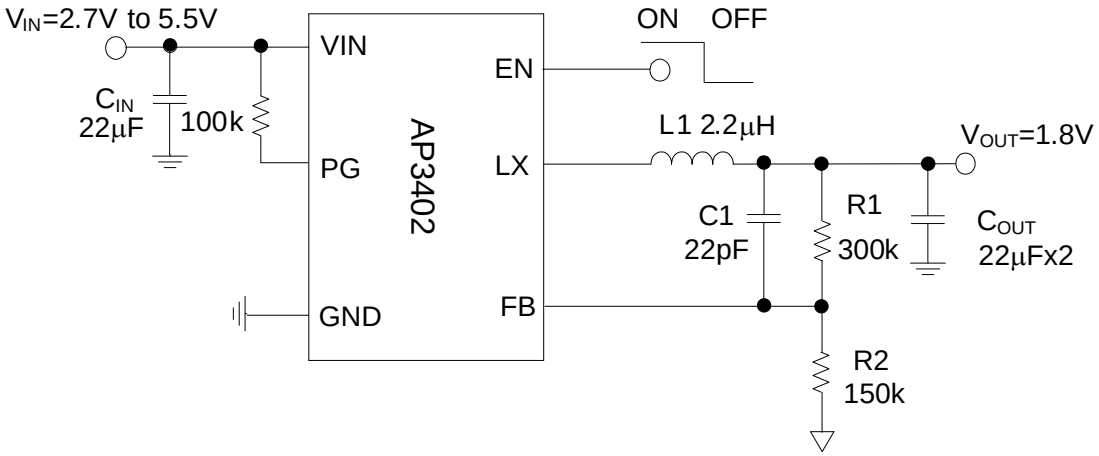
3. Key Features

- Output Current: Up to 2A
- Output Voltage: 0.6V to VIN
- Input Voltage: 2.7V to 5.5V
- Peak Efficiency Up to 95%
- 90μA (Typ) No Load Quiescent Current
- Shutdown Current: <1μA

- 1MHz Switching Frequency
- Internal Soft Start
- No External Compensation Required
- Current Limit Protection
- Thermal Shutdown

4. Applications
   - 5V or 3.3V Point of Load Conversion
   - Telecom/Networking Equipment
   - Set Top Boxes
   - Storage Equipment
   - Video Cards
   - DDR Power Supply

5. Typical Application Schematic



6. Application Information

(1) Setting the output voltage

The output voltage is set using a resister voltage divider from the output to FB. The output voltage is calculated as below:

$$V_{OUT} = 0.6 \times \left(\frac{R_1 + R_2}{R_2} \right)$$

First, select a value for R2, Then, R1 is determined. The output voltage is given by Table1.

Vo	R1	R2	C1
1.0V	100KΩ	150 KΩ	22pF
1.2V	150KΩ	150 KΩ	22 pF
1.5V	225KΩ	150 KΩ	22 Pf
1.8V	300 KΩ	150 KΩ	22 pF
2.5V	317KΩ	100KΩ	22 pF
2.8V	367KΩ	100KΩ	22 pF
3.3V	211KΩ	47 KΩ	22 pF

Table 1: Resistor selection for output voltage setting

(2) Inductor selection

The inductor is used to supply smooth current to output when it is driven by a switching voltage. Its value is determined based on the operating frequency, load current, ripple current, and duty cycle. For most application, the value of the inductor will fall in the range of 2.2uH to 4.7uH. Choose an inductor that has small DC resistance, has enough current rating and is hard to cause magnetic saturation.

(3) Input capacitor

Good quality input capacitor is necessary to filter noise at input voltage source and limit the ripple voltage of input while supplying most of the switch current during the on-time. For input capacitor selection, ceramic capacitor is recommended because they provide both low impedance and small footprint. But tantalum or low electrolytic capacitor is also sufficed.

The important parameters for the input capacitor are the voltage rating and the RMS current rating. The voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a conservative. The RMS of input capacitor current is calculated as:

$$I_{CIN\_RMS} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

I_{CIN_RMS} : The RMS of input capacitor current

As indicated by the RSM ripple current equation, highest requirement for RMS current rating occurs at 50% duty cycle. So the RMS ripple current rating of input capacitor should be greater than half the output current under this worse case. For reliable operation and best performance, ceramic capacitors are preferred for input capacitor because their low ESR and high ripple current rating. And X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristic. Additional, when selecting ceramic capacitor, make sure

it has enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input.

The capacitance of C_{IN} should be more than or equal to10uF

(4) Output capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The output voltage ripple depends directly on the ripple current and it is affected by two parameters from the output capacitor: total capacitance and the equivalent series resistance (ESR). The output ripple voltage can be found from:

$$\Delta V_O = \Delta I_L \times \left[R_{ESR} + \left(\frac{1}{8 \times C_2 \times f_{SW}} \right) \right]$$

ΔV_O: The output ripple voltage

R_{ESR}: The equivalent series resistance of output capacitor

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum capacitor or aluminum electrolytic capacitor are recommended. **The capacitance of C_{OUT} should be more than or equal to 44uF** and the output capacitor voltage rating should be greater than 1.5 times of maximum output voltage.

(5) PCB Layout Guideline

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of the converter and surrounding circuitry by contributing to EMI.

1. power path length

The power path of AP3402/20 includes an input capacitor, output inductor and output capacitor. Place them on the same side of PCB. The GND trace, the SW trance and the VIN trance should be kept short, direct and wide. C_{IN} must be close to Pins VIN and GND. The loop area formed by C_{IN} and GND must be minimized.

2. feedback Net

Special attention should be paid to the route of the feedback wring. The feedback trace should be routed far away from the inductor and noisy power trace. Try to minimize trace length to the FB pin and connect feedback network behind the output capacitors.

3. Via Hole

Be careful to via hole. Via will result high resistance and inductance to the power path. If heavy switching currents must be routed through vias and/or internal planes, use multiple vias parallel to reduce their resistance and inductance. Figure 6 and 7 are example of AP3402 PCB layer.

4. Pad PCB Design

It is recommended that the PCB lead finger pad be designed 0.4mm toe length beyond the package body as a stander to optimize solder volume and extended 0.05mm towards the center line of the package. The dimensions of the thermal pad on the PCB should be equal to the exposed pad on the DFN. The pad must be physically connected to the PCB substrate with solder. Please refer to figure 8.

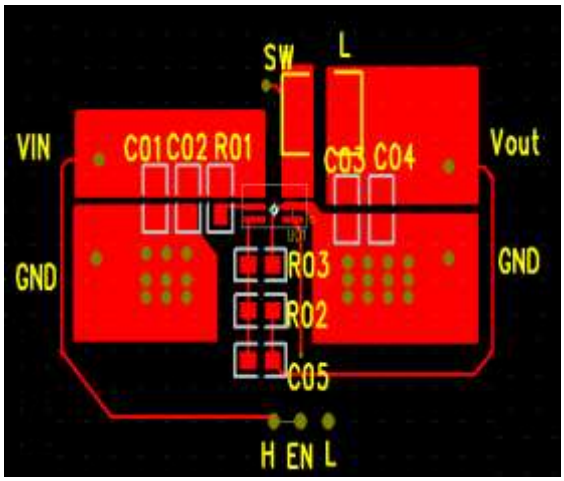


Figure 6: Top Layer

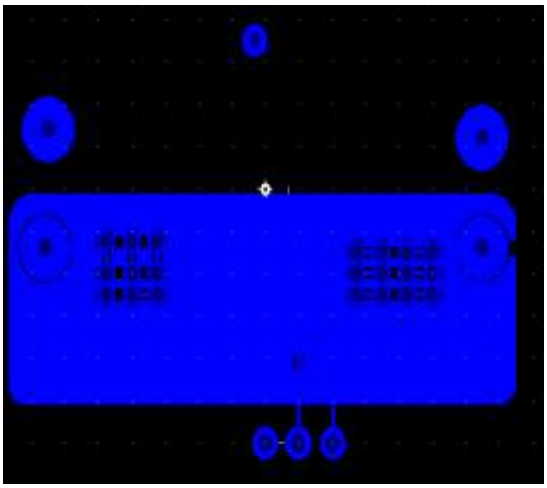


Figure 7: Bottom Layer