AN1140

Active Capacitor Discharge Circuit Considerations for FPGAs

Ian Milne, MOSFET Specialist, Diodes Inc

Summary

FPGA's need the different power rails to be powered up and down in a defined sequence. For power down, each sequenced rail needs to be fully off before the next rail is turned off. With large high speed and high functionality FPGA's, the power rails have large bulk capacitors to be discharged quickly and safely within a total time of 100ms and up to 10 rails each to be discharged within 10ms.

This application note shows a methodology and considerations for safe open ended shutdown to be controlled by a power sequencing circuit and using correctly chosen MOSFET to discharge the capacitor bank.

Introduction

The latest FPGAs found in telecoms equipment, servers and data centers have multiple power rails that need to be correctly sequenced to safely power these systems up and down. Designers of the high reliability DC-DC regulators and FPGA power management need a simple method to safely discharge the large bulk capacitors to avoid damaging the system.

FPGA Power Sequencing

For the latest generation system-on-chip FPGA's, they can have in the order of ten separate power rails supplying the Vcore, memory bus supply, I/O controllers, Ethernet etc. As shown in Figure 1, each rail is supplied by a DC-DC converter to regulate the required voltage supply of 3.3V, 2.5V, 1.8V, 0.9V etc. To power up the system, a particular sequence is followed to ensure safe operation and avoid damaging the system. Likewise during system shutdown, the power sequence is in the reverse order ensuring each power rail is disabled before the next is switched off. This order is controlled via a Power Sequencer chip that enables each DC-DC regulator as per Figure 1.
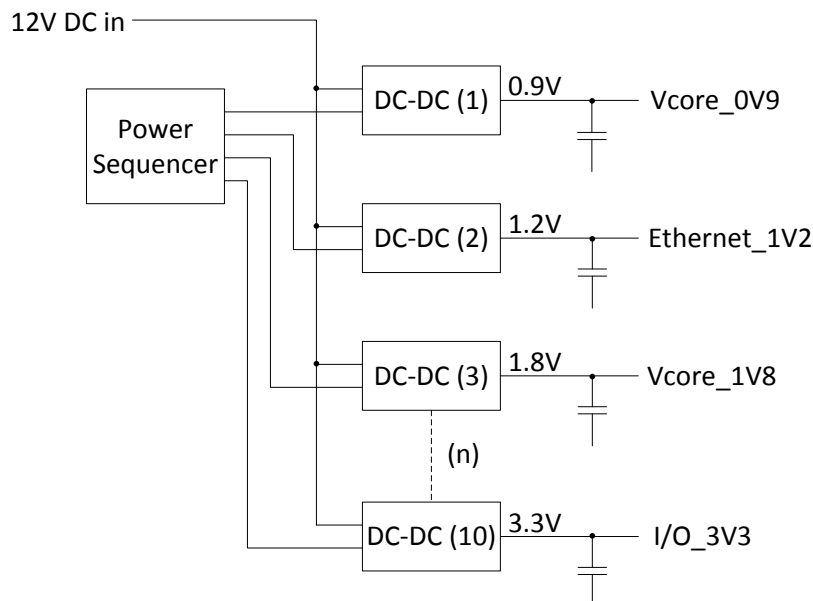

Figure 1 Typical FPGA system power rail supply to each service.

Problems arise when considering the charge stored in the decoupling capacitors on the various power rails. For instance, on the 0.9V Vcore power rail the total decoupling capacitance can be in the order of 10 to 20mF and the residual charge stored in the capacitor bank needs to be actively discharged during power down, before the

next rail in power down sequence is disabled. This avoids violating the power down sequence and protects the FPGA system. For this reason, an active discharge circuit is recommended on each DC-DC regulator output.

Active Capacitor Discharge Switch

By knowing the capacitor bank size, then an open ended method can be implemented to discharge with respect to the RC time constant. The capacitor is assumed to be discharged once the voltage is less than 95% of the charged state which occurs at 3 x RC time constant.

A simple method for doing this is via a switch with a known resistance to ground that can be turned on when discharge is required. Referring to Figure 1, the Power Sequencer enables the output of each DC-DC regulator. This same enable (EN) signal can then be used to feed a switch connected in parallel to the capacitor bank. By inverting the enable signal to drive the switch it will discharge the capacitors as the DC-DC regulator's output is disabled. For the switch, an N-channel Power MOSFET is preferred as it is simple to drive from a logic signal that is referenced to ground. The chosen circuit is detailed in Figure 2 with Q2 as the N-channel Power MOSFET and Q1 as the P-channel MOSFET that inverts the Power Sequencer's EN logic signal.
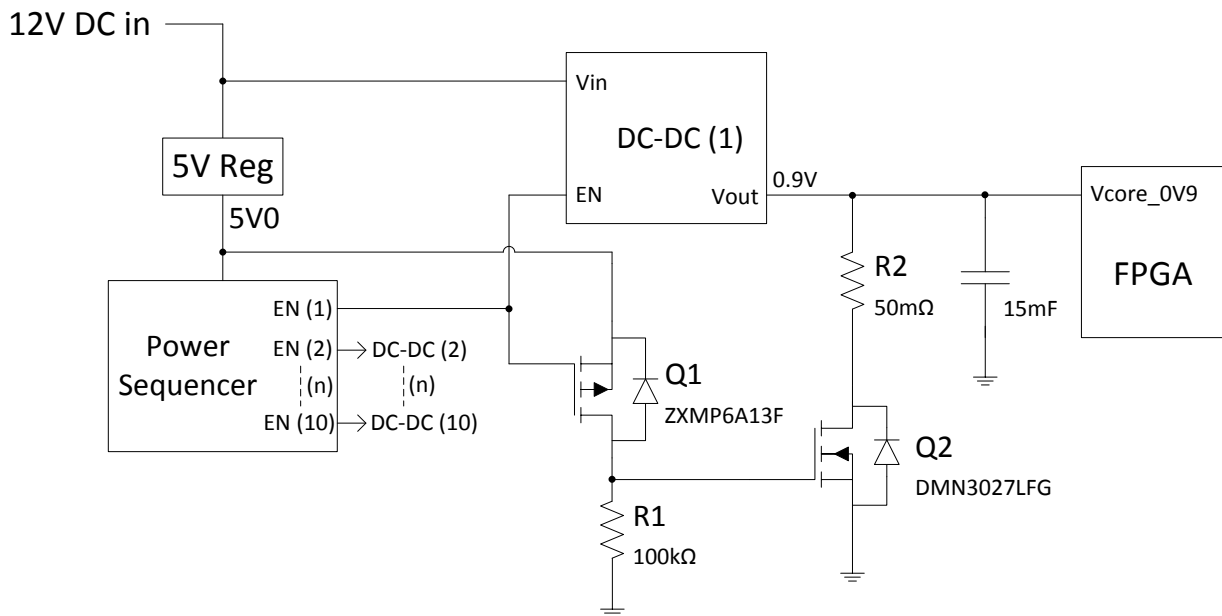

Figure 2 Active Discharge Circuit

Active Capacitor Discharge Circuit Operation

Refer to Figure 2 - the Power Sequencer's EN output feeds both the enable pin on the DC-DC regulator and also the capacitor discharge circuit. When a logic '0' is signalled for shutdown then the P-channel MOSFET (Q1) inverts the signal to then switch on the N-channel MOSFET (Q2) to discharge the capacitor bank.

The discharge circuit assumes the DC-DC regulator cannot continue producing an output once the shutdown signal is applied. If there is power available from the DC-DC regulator's output after the shutdown command is activated, then a delay must be introduced before the discharge circuit is activated. This is to ensure the discharge MOSFET does not try to sink the full output current capability of the DC-DC regulator.

To enhance the N-channel Power MOSFET (Q2) from a logic '0' signal then a P-channel MOSFET (Q1) inverts the signal to a 5V to apply across the Q2 gate-source. The P-channel MOSFET (Q1) is chosen to not have a low gate threshold voltage ($V_{GS(th)}$). This is because $V_{GS(th)}$ falls with respect to temperature and Q1 needs to be in the OFF state during logic '1' state to avoid false turn-on of Q2. An optimum value suitable for 5V operation in conjunction with the Power Sequencer needs to be selected.

With logic '1' output from the Power Sequencer, then the DC-DC regulator is enabled in the ON state, and Q2 must be in the OFF state. Taking the logic '1' output with a minimum high-level output voltage of 4.19V (Spec of Power Sequencer's EN pin output), then the Q1 $V_{GS(th)}$ needs to be greater than 0.9V at ambient operating temperature of 60°C. Further to this, the gate of Q2 needs pulling down to source potential via R1 resistor of 100kΩ to avoid false turn-on.

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The $V_{GS(th)}$ variation over temperature is found in the typical electrical curves of MOSFET datasheets. For example the normalised $V_{GS(th)}$ vs temperature for the ZXMP6A13F is given in Figure 3. The ZXMP6A13F is the preferred device as the guaranteed minimum $V_{GS(th)}$ is 1V at room temperature falling to about 0.9V at 60°C.
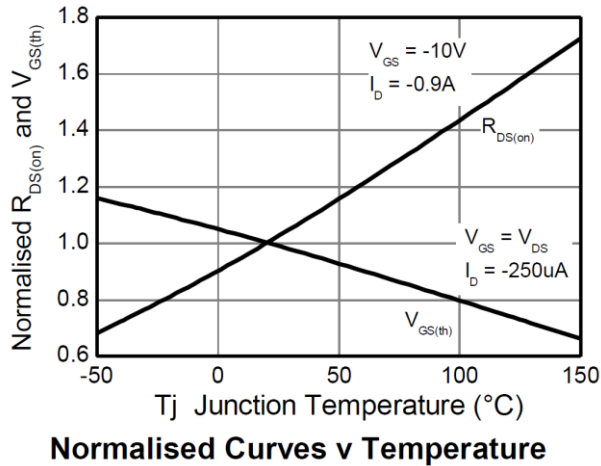

Normalised Curves v Temperature

Figure 3 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ curves over temperature for the ZXMP6A13F

When the Power Sequencer enable output goes to logic '0', then the maximum low-level output of 0.270V is present and Q1 needs to guarantee that the channel is enhanced with this 5V – 0.270V signal to ensure that Q2 turns-on and discharges the capacitor bank. Therefore Q1 needs to have an on-state at V_{GS}=-4.5V.

To discharge the capacitor bank, an N-channel Power MOSFET (Q2) is chosen to have an on-resistance ($R_{DS(on)}$) suitable to discharge the largest capacitance bank, within 10ms to ensure full shutdown sequence of discharging 10 channels occurs in less than 100ms. An auxiliary power supply must be provided to drive the shutdown circuit (Power Sequencer) for at least 100ms after power down has been activated.

Time to discharge calculation

Using a 3 x RC time constant where R is the combined resistance of the ESR of the capacitor bank (assumed to be < 5mΩ), the parasitic trace resistance (assumed to be < 5mΩ), a series drain resistor (R2) and the Power MOSFET Q2 $R_{DS(on)}$. Also included is the temperature dependency of the Power MOSFET on-resistance that can be as high as 1.5x the maximum $R_{DS(on)}$ at T_{amb} = 25°C, whilst assuming the junction has reached the absolute maximum temperature rating (typical $T_{J(max)}$ = 150°C) – refer to Figure 5

To discharge the 15mF capacitor bank in less than 10ms, a 3 x RC = 8ms is required:

3 x (10mΩ + R2 + (1.5 x $R_{DS(on)}$)) x 15mF = 8ms

Therefore the Power MOSFET Q2 needs an $R_{DS(on)}$ < 80mΩ at V_{GS} = 4.5V, T_{amb} = 25°C. This is assuming a 50mΩ series drain resistor, referred to as R2 in Figure 2, is used in conjunction with the MOSFET; reasoning explained on the next page.

Safe Operating Area and Transient Thermal Stress

The Power MOSFET Q2 is chosen to have a power rating capable of handling the transient power dissipation of the discharge current. Peak power is calculated via simulation and the value checked against the transient power capability graphs of the Power MOSFET datasheet. As the Power MOSFET will be dissipating the capacitor's energy as a function of both current and voltage over time then the Safe Operating Area (SOA) curve in the datasheet needs to be reviewed. This will give the maximum single pulse that the Power MOSFET can safely handle whilst ensuring the junction temperature does not exceed the absolute maximum rating, typical $T_{J(max)}$ = 150°C. A SOA should be based on the application's ambient operating temperature with the required MOSFET gate drive, in this instance 4.5V. In the case of discharging the 0.9V charged capacitor bank, then review the SOA curve for single pulse peak current capability at 1V between 1ms and 10ms pulse width curves. The SOA should be for a typical application ambient temperature, which is assumed to be 60°C, whilst mounted on a PCB with minimal heatsinking, otherwise known as minimum recommended pad (MRP) layout. Refer to Figure 4 for the SOA of the DMN3027LFG under these conditions.
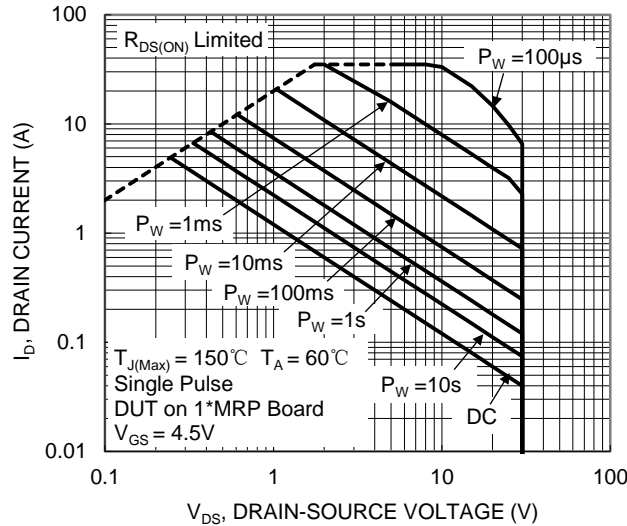
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Figure 4 Safe Operating Area (SOA) for DMN3027LFG

The peak surge current from the capacitor bank needs to be measured in the actual circuit to ensure that sufficient resistance is slowing down the response to avoid sharp rising current peaks that could cause EMI issues and also transient thermal stress on both the N-channel Power MOSFET and capacitor bank. In Figure 2, a 50mΩ series resistor is added to the drain of Q2 to ensure that a fixed known value (temperature independent) dominates the total resistance in the discharge path.

MOSFET On-Resistance Variation

Beware that the on-resistance of a MOSFET varies over temperature, as shown in Figure 5, with as much as 15mΩ variation over the expected operating temperature range at the 4.5V gate drive. On top of this you will also have $R_{DS(on)}$ variation from part-to-part and lot-to-lot. The typical $R_{DS(on)}$ is 22mΩ with a maximum spec limit of 26mΩ for the 4.5V gate drive on the DMN3027LFG at room temperature.

Typical On-Resistance vs. Drain Current and Temperature

On-Resistance Variation with Temperature
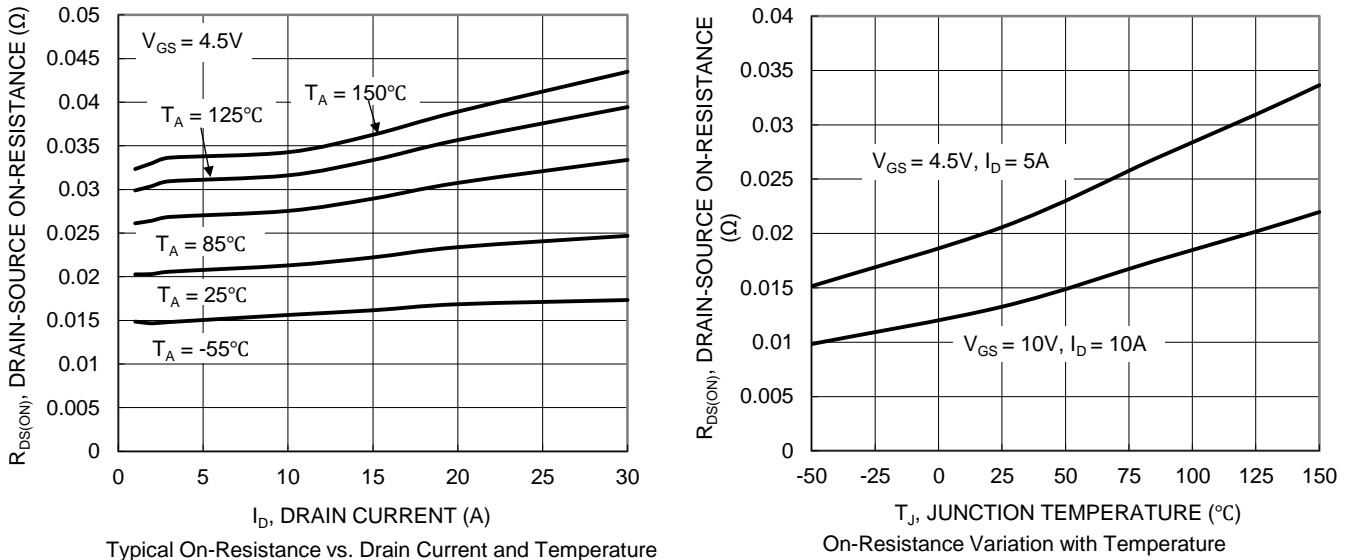
Figure 5 On-resistance temperature response of DMN3027LFG

Therefore to ensure a known resistance dominates the discharge path it is best practice to use an R2 series resistor that is about double the max $R_{DS(on)}$ at the chosen gate drive. With R2 of 50mΩ and $R_{DS(on)}$ varying from 15mΩ to 40mΩ (typ. 22mΩ), gives a 95% discharge time of 3.9 to 5.4ms (3x RC). This is with a worst case capacitor bank size of 20mF.

Power Dissipation

Calculating the power dissipation in both the Power MOSFET Q2 and the series resistor R2 depends on the duty cycle and period of when Q2 is turned on.

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If the 0.9V output on the DC-DC regulator was enabled whilst Q2 is turned on, then up to 11W could be across Q2 and R2. This is assuming the junction temperature reaches 150°C and the typical $R_{DS(on)}$ stabilises at 35mΩ for 11A as shown in Figure 5. This scenario should not be permitted as it violates the maximum power dissipation in the DMN3027LFG and causes the junction temperature to exceed the absolute maximum ratings. Therefore the DC-DC regulator output must be disabled whilst the Q2 is enabled.

This means that the worst case scenario will be caused by charging and discharging the capacitor for short periods of time. Assuming that the Power Sequencer goes into a continuous loop of enabling and then disabling the DC-DC regulator every 20ms (10ms enable + 10ms disable), then that would cause about 0.5W power across Q2 and R2. This is calculated by knowing the total energy stored in the capacitor bank will be discharged every 20ms:

$P = E / t = \frac{1}{2}CV^2 / 20ms = 500mW$, taking C = 20mF for largest capacitor bank charged to 1V.

With the worst case $R_{DS(on)}$ being 40mΩ from 26mΩ x 1.5 at V_{GS} = 4.5V, $T_{J(max)}$ = 150°C (From Figure 3). Therefore power dissipation in Q2 and R2 is 222mW and 278mW, respectively. The lowest $R_{DS(on)}$ of 15mΩ would increase the power dissipation in R2 to 385mW; meaning that a surface mounted resistor of 0.5W rating.

In the typical application, the ambient temperature is expected to reach 60°C and the DMN3027LFG has an $R_{\theta JA}$ = 130°C/W on minimum recommended pad layout, then T_J reaches 90°C when dissipating 222mW. This gives plenty of headroom from the $T_{J(max)}$ = 150°C.

Measurements in Discharging a Capacitor Bank

A capacitor bank using 6x 2,200uF electrolytic capacitors (13.2mF) was assembled using DMN3027LFG and ZXMP6A13F as per Figure 2. The ZXMP6A13F was manually triggered with a 5V signal.

The measurements were conducted with and without a 50mΩ series resistor, and then at room, sub-zero and elevated temperatures to observe the change in peak current and discharge time. Discharging through the DMN3027LFG channel $R_{DS(on)}$ resistance only (without 50mΩ) creates the worst case scenario for observing the maximum peak currents. Note in the following curves that the timescales are different – 200µs/div and 1ms/div

Channel 1 (C1) is in yellow =   Voltage on DMN3027LFG gate pin
Channel 3 (C3) is in magenta =   Voltage on capacitor bank
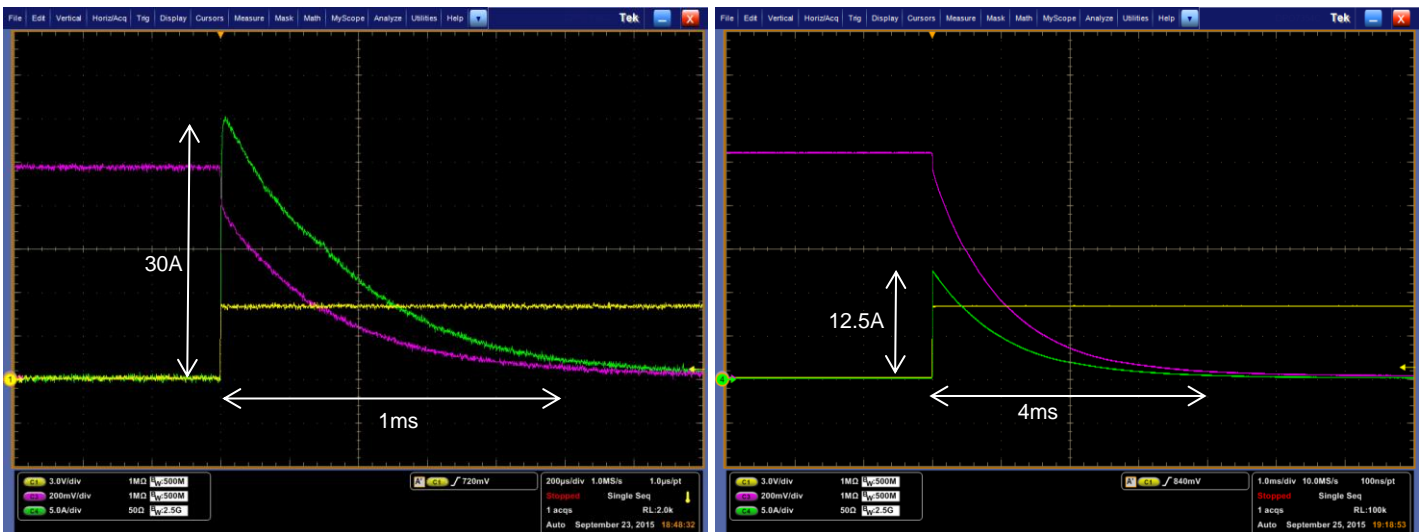Channel 4 (C4) is in green =   Current probe from DMN3027LFG source pin

Figure 6 Room temperature measurements (approx. Ta=20°C).
Left curves = 30A peak current discharge through DMN3027LFG channel resistance only (200µs/div)
**Right curves = 12.5A peak current discharge through DMN3027LFG and 50mΩ series resistor (1ms/div)**

Refer to Figure 6, Figure 7 and Figure 8 - discharging a 13.2mF capacitor bank via only the DMN3027LFG generates a peak current varying from 24A to 35A depending on the temperature response of the MOSFET's $R_{DS(on)}$. By adding in a 50mΩ series resistor, this limits both the peak current to <15A and the variation over temperature only 11A to 14A. Note that as temperature rises the peak current falls with respect to the $R_{DS(on)}$ increasing.

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Discharge time to 95% of the initial 1V charged state occurs in about 3 to 4ms even with varying temperature. This is as expected from the 3x RC time constant and similar results are replicated by SPICE modelling this circuit - refer to the Appendices. Simulating a 13.2mF capacitor bank at 27°C (default), with a 50mΩ series resistor added in, then peak current is about 13A and it discharges to 95% within 3ms.

Figure 7 Elevated temperature measurements (approx. Ta=70°C).
Left curves = 24A peak current discharge through DMN3027LFG channel resistance only (200µs/div)
Right curves = 11A peak current discharge through DMN3027LFG and 50mΩ series resistor (1ms/div)

Figure 8 Sub-zero temperature measurements (approx. Ta=-20°C).
Left curves = 35A peak current discharge through DMN3027LFG channel resistance only (200µs/div)
Right curves = 14A peak current discharge through DMN3027LFG and 50mΩ series resistor (1ms/div)

Conclusion

A safe and simple method to discharge large capacitor banks based on the known RC time constant has been demonstrated. This open ended technique can be scaled with respect to the capacitance size. The following devices have been chosen:

Q1 = ZXMP6A13F   P-channel MOSFET in SOT23
Q2 = DMN3027LFG   N-channel MOSFET in PowerDI3333-8
R2 = 50mΩ   Surface mount resistor able to dissipate 500mW.

By adding in a 50mΩ series resistor in the discharge path, this limits the peak discharge current and stabilises the variation over temperature. Both the measured and simulated results are in good agreement; giving designer's confidence in modelling different capacitor bank sizes.

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Appendices - Simulation using SPICE models in Diodes Inc Circuit Simulator (SIMetrix)

MOSFET spice models are provided on the following page and the SIMetrix circuit is embedded as an attached file. Open the SIMetrix file within Adobe, by clicking the paper clip icon on the left (Attachments).
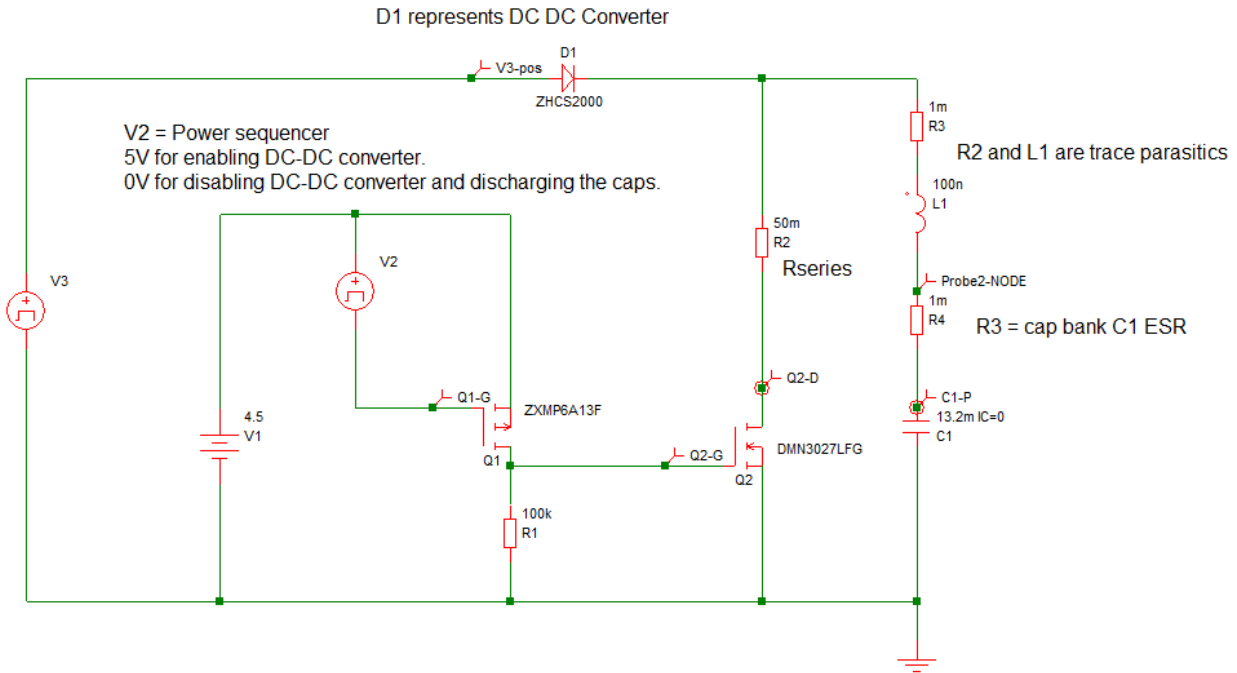
Signal	Description
V3-pos / V	DC-DC Converter Modules Output Voltage
I(C1-P) / A	Capacitor bank charge and discharge current
Q1-G / V	Inverted enable signal from Q1 to gate of Q2.
Q2-G /V	Shut down /power up enable signal from Power Rail Sequencer to Q1 (PMOS)
Probe2-Node / mV	C1 capacitor bank voltage
Power (Q2) /W	Power in Power MOSFET (Q2) during discharge period

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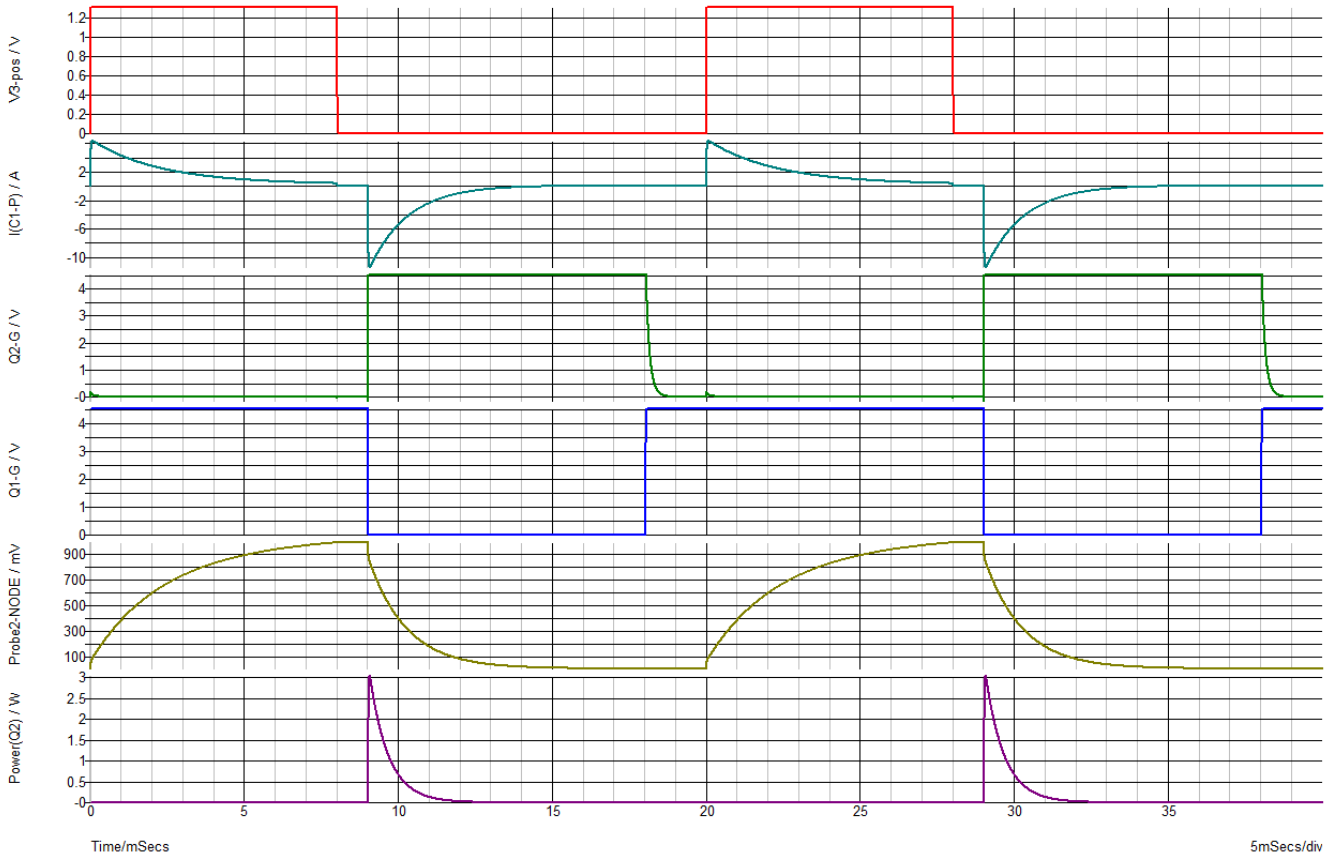
MOSFET SPICE models are:

```
*---------- DMN3027LFG Spice Model ----------
.SUBCKT DMN3027LFG 10 20 30
*     TERMINALS: D  G  S
M1 1 2 3 3 NMOS  L = 1E-006  W = 1E-006
RD 10 1 0.006868
RS 30 3 0.001
RG 20 2 1.92
CGS 2 3 5.089E-010
EGD 12 0 2 1 1
VFB 14 0 0
FFB 2 1  VFB 1
CGD 13 14 4.8E-010
R1 13 0 1
D1 12 13  DLIM
DDG 15 14  DCGD
R2 12 15 1
D2 15 0  DLIM
DSD 3 10  DSUB
.MODEL NMOS NMOS  LEVEL = 3  VMAX = 1E+005  ETA = 0.001  VTO = 2.23
+ TOX = 6E-008  NSUB = 1E+016  KP = 33.14  U0 = 400  KAPPA = 0.001011
.MODEL DCGD D  CJO = 2.68E-010  VJ = 0.204  M = 0.3131
.MODEL DSUB D  IS = 1.168E-010  N = 1.244  RS = 0.00323  BV = 35  CJO = 1.898E-010  VJ = 0.2902  M =
0.4412
.MODEL DLIM D  IS = 0.0001
.ENDS
*Diodes DMN3027LFG Spice Model v1.0 Last Revised 2015/05/28


*---------- ZXMP6A13F Spice Model ----------
.SUBCKT ZXMP6A13F 30 40 50
*          D G S
M1 6 2 5 5 Pmod L=1.2E-6 W=0.39
M2 5 2 5 6 Nmod L=1.4E-6 W=0.195
RG 4 2 3
RIN 2 5 1E9
RD 3 6 Rdmod 0.25
RL 3 5 3E9
C1 2 5 25E-12
C2 3 4 15E-12
D1 3 5  Dbodymod
LD 3 30 0.5E-9
LG 4 40 1.0E-9
LS 5 50 1.0E-9
.MODEL Pmod PMOS (LEVEL=3 TOX=5.5E-8 NSUB=1e16
+VTO=-1.5 KP=6e-6 RS=0.005 NFS=12e11 KAPPA=0.01 UO=650 IS=1E-15 N=10)
.MODEL Nmod NMOS (LEVEL=3 TOX=5.5E-8 NSUB=1E16
+TPG=-1 IS=1E-15 N=10)
.MODEL Dbodymod D (IS=1e-11 RS=0.05 IKF=0.001966 XTI=-1 TRS1=1.2e-3
+CJO=3.514e-11  BV=66)
.MODEL Rdmod RES (TC1=5e-3 TC2=1e-5)
.ENDS ZXMP6A13F
*ZETEX ZXMP6A13F Spice Model v2.0 Last Revised 15/02/05
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