AN1170

DGD0215 DGD0216 and DGD0211C Application Information

The DGD0215/16 and DGD0211C are High-Speed, Low-Side Gate Drivers, capable of source current of 1.9A and sink current of 1.8A. Low-Side Gate Drivers will optimally charge the gate of MOSFETs or IGBTs in a ground-based configuration. Below (Figure 1) is an example application using the DGD0216 with an IGBT in a PFC application; the aim of the DGD0216 is to optimally drive Q1 by quickly providing a charge on the gate when OUT becomes high. Typical PWM from the PFC control is 3.3V and the DGD0215/16 and DGD0211C convert the 3.3V to the value of VCC, often 12V. Because of its high-speed performance, the DGD0216/16 and DGD0211C are also well-suited for low voltage power supplies. In this discussion, the important parameters needed to design in the DGD0215/16 and DGD0211C are discussed: Gate Driver component selection, decoupling capacitor discussion, and PCB layout suggestions.

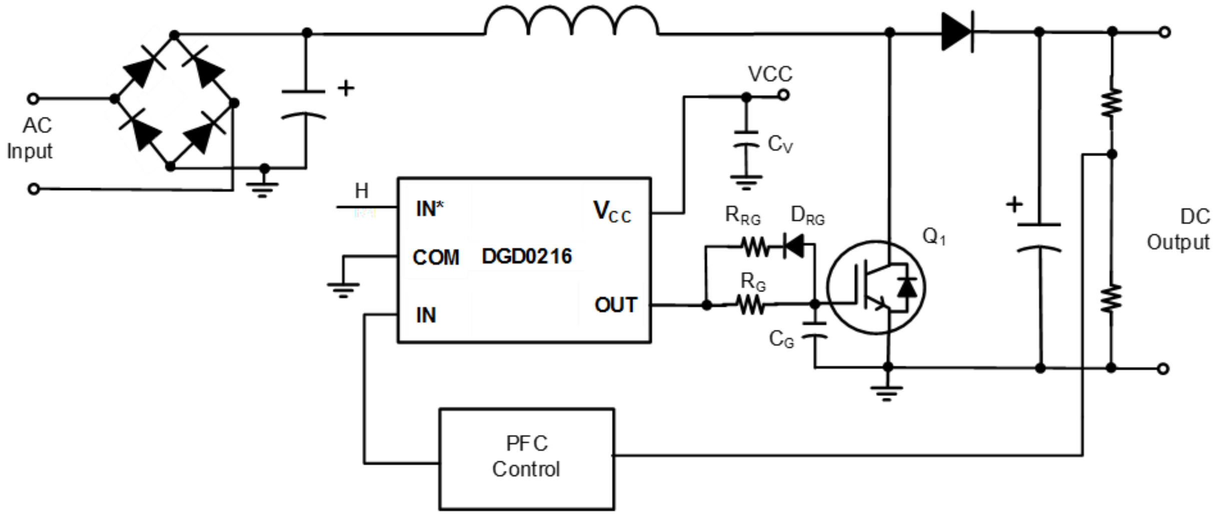

Figure 1. PFC application example using Low-Side Gate Driver DGD0216

Gate Component Selection

The most crucial time in the gate drive is the turn on and turn off of the IGBT; the aim is to perform this function quickly, but with minimal noise and ringing when the IGBT turns on. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the IGBT.

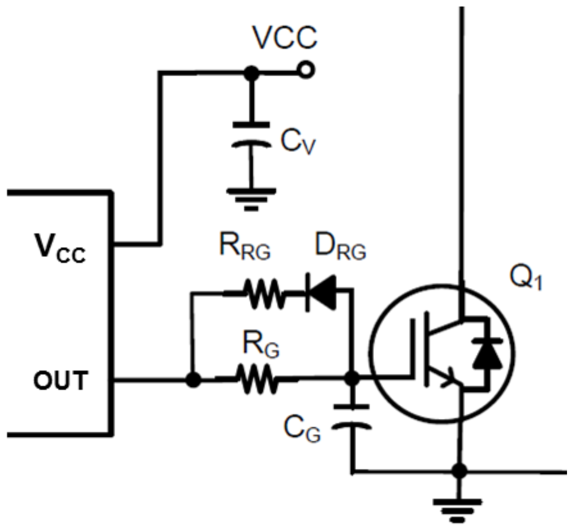

Figure 2. Gate Drive components for DGD0216

Considering the Gate Driver components for the DGD0216 in Figure 2, with the careful selection of R_G and R_{RG}, it is possible to selectively control the rise time and fall time of the gate drive to the IGBT. For turn on, all current will go from the IC through R_G and charge the IGBT gate capacitance, hence increasing or decreasing R_G will increase or decrease rise time in the application. With the addition of D_{RG}, the fall time can be separately controlled as the turn off current flows from the IGBT gate capacitance, through R_{RG} and D_{RG} to the driver in the IC to GND. So, increasing or decreasing R_{RG} will increase or decrease the fall time. Sometimes finer control is not needed and only R_G needs to be used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, contrasted with a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. R_G values are typically between 5Ω and 50Ω, optimal value decided by IGBT gate capacitance and drive current of gate driver. R_{RG} values are typically between 3Ω and 20Ω, optimal value decided by IGBT gate capacitance and drive current of gate driver.

The gate to source capacitor C_G is also used to minimize ringing and noise and to provide overall stability if the gate driver and IGBT are not the optimal match. Most systems will not need C_G (increasing the gate resistor can decrease ringing and provide system stability) but if required, then C_G = 1nF is a good typical value.

V_{cc} Decoupling Capacitors

For optimal operation, V_{CC} decoupling is crucial for all Gate Driver ICs. With poor decoupling, larger V_{CC} transients will occur at the IC when switching.

As shown in Figure 2, C_V is the decoupling capacitor. C_V is used to decouple faster edge changes to V_{CC} and should be a low ESR ceramic capacitor placed close to the V_{CC} pin (see Layout section). This component provides stability when V_{CC} is quickly pulled down with load from the IC; typical values are 0.1µF to 1µF.

Inputs and Device Response

The inputs of the DGD0215, DGD0216 and the DGD0211C, and the input to output function, are the main difference between the three Low- Side Gate Drivers. Below, the inputs and input to output response are described for each device.

For the DGD0215/16, the IC PWM inputs, IN and IN*, are very high impedance inputs with a pull-down resistor for IN and a pull-up resistor for IN*. The pull-up and pull-down resistors on IN* and IN have an approximate value of 1MΩ (see Figure 3).

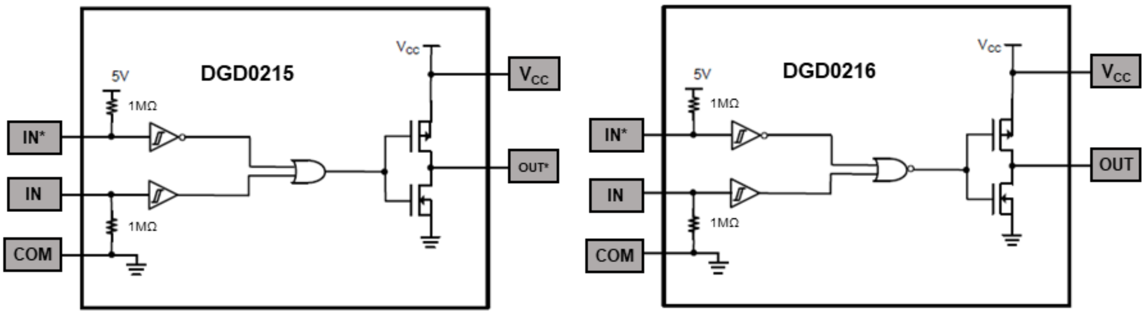

Figure 3. Input logic and functional block diagram for DGD0215 and DGD0216.

The DGD0215/16 is typically used by driving one input and keeping the other input in a known state. To drive the PWM on the IN pin, and for best noise performance, it is suggested to connect the IN* directly to H (see Figure 1, i.e. 3.3V or 5.0V). To drive the PWM on the IN* pin, and for best noise performance, it is suggested to connect the IN pin directly to GND. The table shown in Figure 4 indicates the input/output response table of the DGD0215/16.

IN	IN*	DGD0215 (OUT*)	DGD0216 (OUT)
H	H (open)	L	H
L	H (open)	H	L
L (open)	H	H	L
L (open)	L	L	H

Figure 4. Input/output response table for the DGD0215 and DGD0216.

For the DGD0211C, the IC PWM inputs, IN and IN*, are also very high impedance inputs with a pull-up resistor for IN and a pull-down resistor for IN*. The pull-up and pull-down resistors on IN* and IN also have an approximate value of 1MΩ (see Figure 5). The table shown in Figure 6 indicates the Input/Output relationship of the DGD0211C; when the inputs of the DGD0211C are open, the output is high (to V_{CC}).

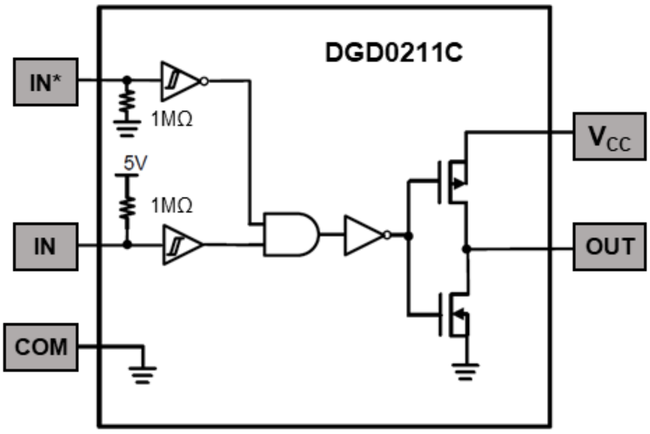

Figure 5. Input logic and functional block diagram for the DGD0211C.

IN	IN*	OUT
0	0	0
0	1	0
1	0	1
1	1	0

Figure 6. Input/output response table for the DGD0211C.

Matching Gate Driver with MOSFET or IGBT

IC drive current and MOSFET/IGBT gate charge

Gate Driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD0215/16 and DGD0211C the source and sink drive current is I_{O+} = 1.9A and I_{O-} = 1.8A.

For a given MOSFET/IGBT, with the known drive current of the DGD0215/16 and DGD0211C, you can estimate how long it will take to turn on/off the MOSFET/IGBT with the equation:

$t = Q_g / I$

Q_g = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current

For example, consider the Diodes' DMN3009SK3, 30V 20A, Q_g = 42nC; with the DGD0215/16 and DGD0211C I_{O+} = 1.9A then t_r = 22ns, and for I_{O-} = 1.8A, t_f = 23ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also, the addition of a gate resistor will increase the t_r and t_f.

PCB layout suggestions

Layout also plays a considerable role since unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 7 shows the DGD0215/16 and DGD0211C with parasitic inductances in the high current path (L_{P1}, L_{P2}) which would be caused by inductance in the metal of the trace. Considering Figure 7, the length of the tracks in red should be minimized and the decoupling capacitor (C_V) should be placed as close to the IC as possible as well as using low ESR ceramic capacitors. And finally, the gate resistor (R_G) should be a surface mount device. These suggestions will reduce the parasitics due to the PCB traces.

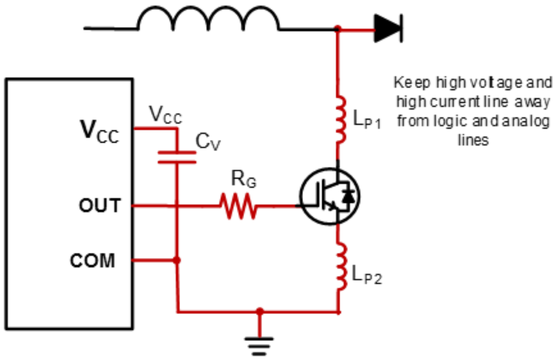

Figure 7. Layout suggestions for DGD0215/16 and DGD0211C, tracks in red should be as short as possible

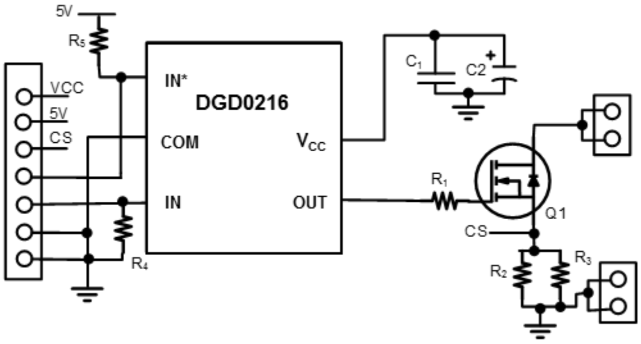

Figure 8. Schematic for layout example of DGD0216 shown in Figure 9.

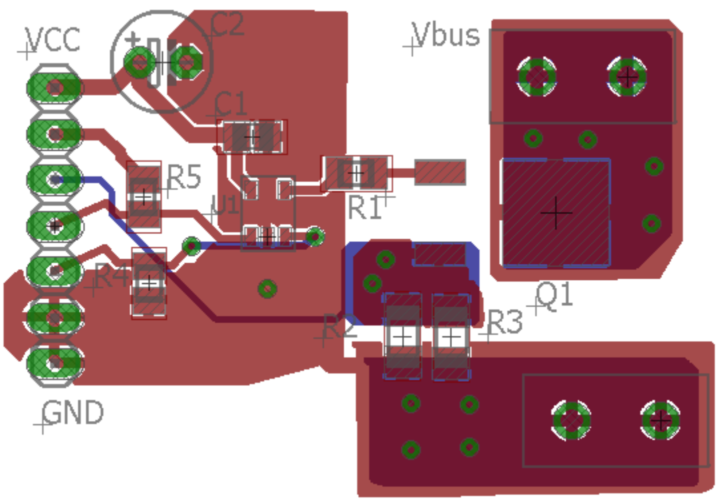

Figure 9. Layout of the schematic shown in Figure 8.

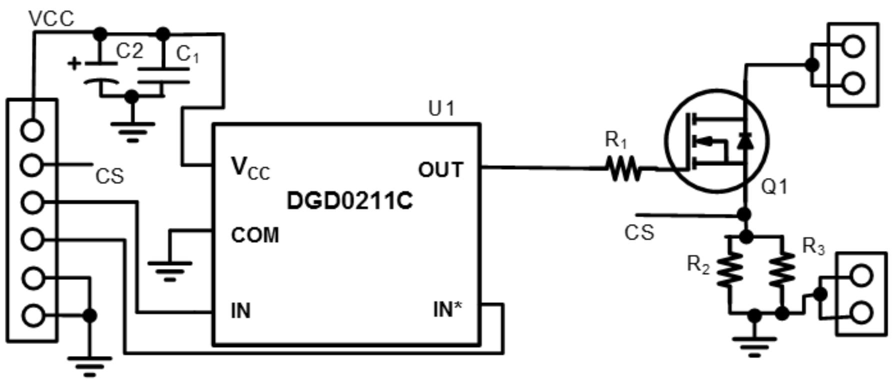

Figure 10. Schematic for layout example of DGD0211C shown in Figure 11.

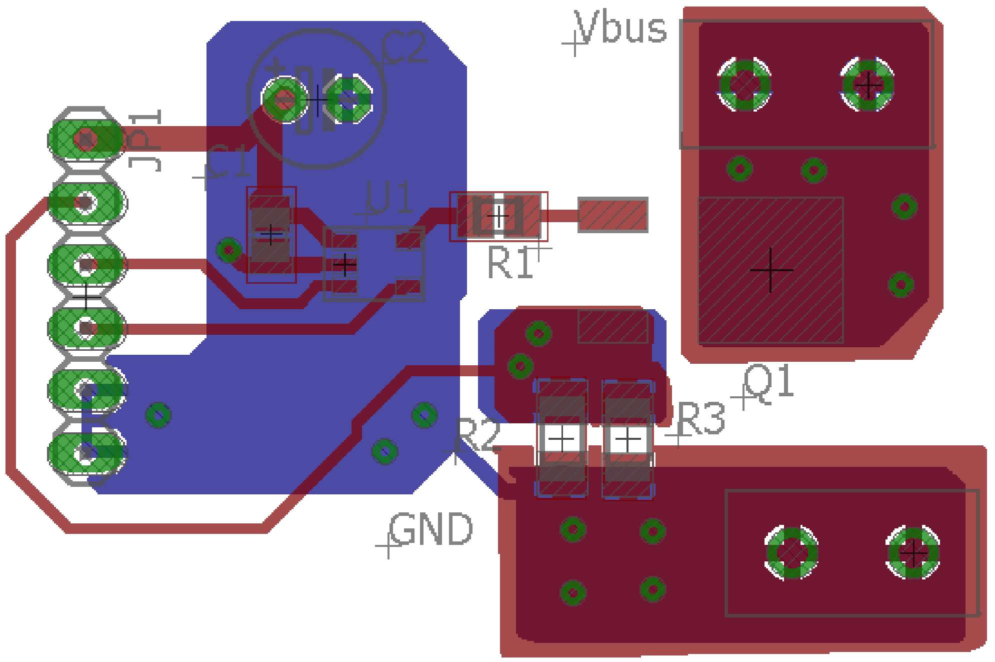

Figure 11. Layout example of the DGD0211C, schematic shown in Figure 10.

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