AN1171

DGD0227 Application Note

The DGD0227, Dual 4.0A High-Speed Low-Side Gate Driver is used to optimally drive the gate of MOSFETs or IGBTs in a ground-based configuration. Below (Figure 1) is an example application using the DGD0227 with an IGBT in a PFC application; the aim of the DGD0227 is to optimally drive Q1 by quickly providing a charge on the gate when OUTA becomes high. Typical PWM from the PFC control is 3.3V and the DGD0227 converts the 3.3v to VCC, usually 12V. Because of its high-speed performance, the DGD0227 is also well suited for low voltage power supplies. In this discussion, the important parameters needed to design in the DGD0227 are discussed: Gate Driver component selection, decoupling capacitor discussion, and PCB layout suggestions. Below, only one channel of the DGD0227 is being used; the second channel can also be used to drive another ground based IGBT, as they are independently functioning channels.

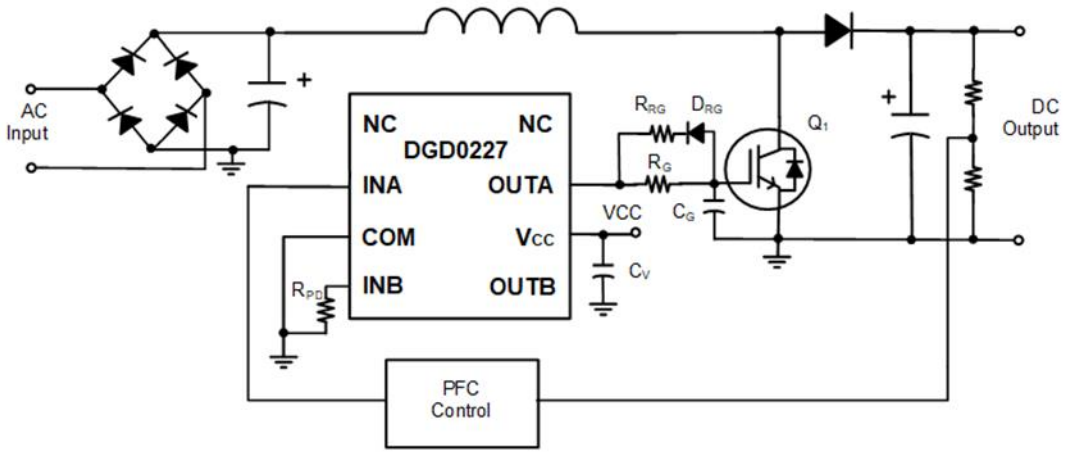

Figure 1. PFC application example using DGD0227

Gate Component Selection

The most crucial time in the gate drive is the turn on and turn off of the IGBT; the aim is to perform this function quickly, but with minimal noise and ringing when the IGBT turns on. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the IGBT.

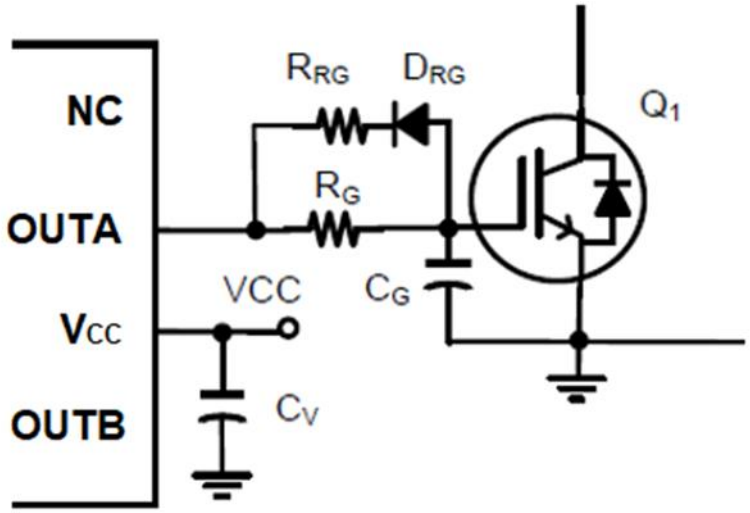

Figure 2. Gate Drive components for DGD0227

Considering the Gate Driver components for the DGD0227 in Figure 2, with the careful selection of R_G and R_{RG} , it is possible to selectively control the rise time and fall time of the gate drive to the IGBT. For turn on, all current will go from the IC through R_G and charge the IGBT gate capacitance, hence increasing or decreasing R_G will increase or decrease rise time in the application. With the addition of D_{RG} , the fall time can be separately controlled as the turn off current flows from the IGBT gate capacitance, through R_{RG} and D_{RG} to the driver in the IC to GND. So increasing or decreasing R_{RG} will increase or decrease the fall time. Sometimes finer control is not needed and only R_G is required.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistor values. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, contrasted with a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. R_G values are typically between 5Ω and 50Ω, the optimal value decided by IGBT gate capacitance and drive current of Gate Driver. R_{RG} values are typically between 3Ω and 20Ω, the optimal value decided by IGBT gate capacitance and drive current of Gate Driver.

The gate to source capacitor C_G is also used to minimize ringing and noise and to provide overall stability if the Gate Driver and IGBT are not the optimal match. Most systems will not need C_G (increasing the gate resistor can decrease ringing and provide system stability) but if required, then C_G=1nF is a good typical value.

V_{cc} Decoupling Capacitors

For optimal operation, V_{CC} decoupling is crucial for all Gate Driver ICs. With poor decoupling, larger V_{CC} transients will occur at the IC when switching.

As shown in Figure 2, C_V is the decoupling capacitor. C_V is used to decouple faster edge changes to V_{CC}, and should be a low ESR ceramic capacitor placed close to the V_{CC} pin (see Layout section). This component provides stability when V_{CC} is quickly pulled down with load from the IC; typical values are 0.1µF to 1µF.

Input Resistors

The IC PWM inputs, INA and INB, are very high-impedance inputs with pull-down resistors; The pull-down resistors on INA and INB have an approximate value of 250kΩ (see Figure 3).

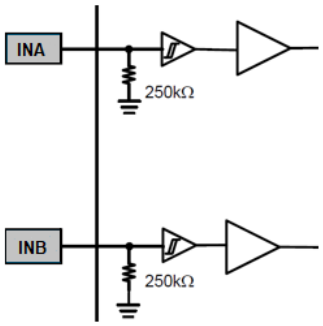

Figure 3. Input Logic for DGD0227

When looking at Figure 1, there is a pull-down resistor on INB (RPD); it is suggested if there are unused inputs, a pull-down resistor (5kΩ to 10kΩ) be used on the unused pin to have superior noise performance.

Matching Gate Driver with MOSFET or IGBT

IC drive current and MOSFET/IGBT gate charge

Gate Driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD0227, the drive current is I_O=4A typical.

For a given MOSFET/IGBT, with the known drive current of the DGD0227, you can calculate how long it will take to turn on/off the MOSFET/IGBT with the equation:

t = Qg/I

Qg = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current

For example with the Diodes' DMN3009SK3, 30V IGBT, Qg = 42nC; and with the DGD0227 I_O=4A, tr/tf = 11ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also, an addition of a gate resistor will increase the tr and tf.

PCB layout suggestions

Layout also plays a considerable role since unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 4 shows the DGD0227 with parasitic inductances in the high current path (L_{P1}, L_{P2}) which would be caused by inductance in the metal of the trace. Considering Figure. 4, the length of the tracks in red should be minimized, and the decoupling capacitor (C_V) should be placed as close to the IC as possible as well as using low ESR ceramic capacitors. And finally, the gate resistor (R_G) should be a surface mount device. These suggestions will reduce the parasitics due to the PCB traces.

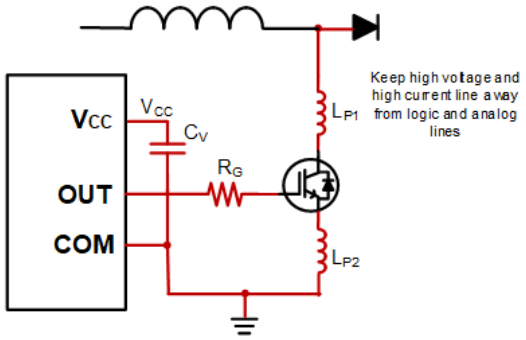

Figure 4. Layout suggestions for DGD0227, lines in red should be as short as possible.

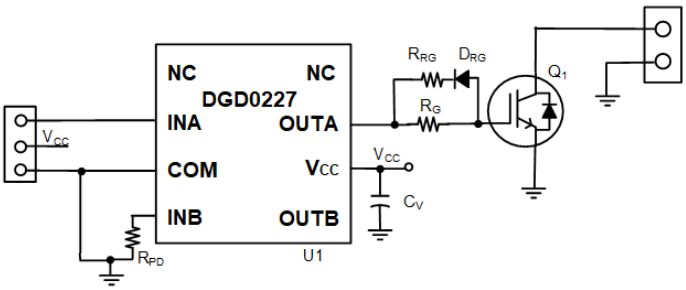

Figure 5. Schematic for layout example in Figure 6.

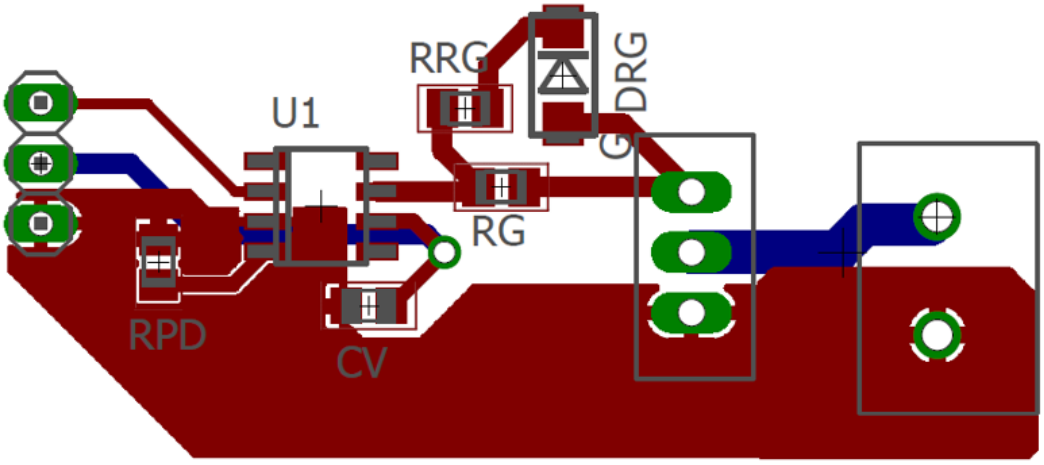

Figure 6. Layout of the schematic shown in Figure 5, DGD0227 in SOIC8.

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