AN1175

DGD2110 DGD2113 Application Note

The DIODES™ DGD2110/2113 are High Side/Low Side gate drivers used to optimally drive the gate of MOSFETs or IGBTs. For the DGD2110, the high-side floating well has a maximum operation of 500V; and for the DGD2113, the high-side floating well has a maximum operation of 600V. Below (Figure 1) is an example application using the DGD2110 with MOSFETs as part of the power switching in the primary side of a full bridge converter. In this discussion, the important parameters needed to design in the DGD2110/2113 are discussed; main sections are bootstrap resistor, diode, and capacitor selection, gate driver component selection, decoupling capacitor discussion, and PCB layout suggestions.

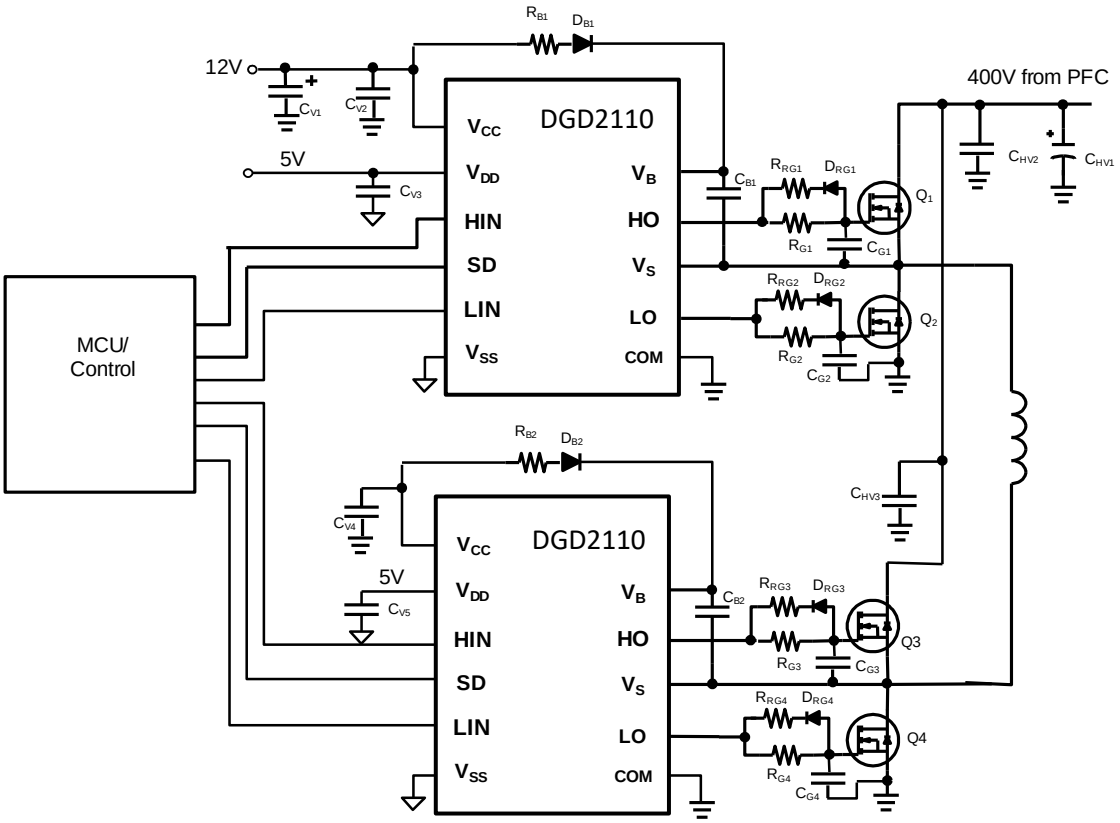

Figure 1. Primary side of full bridge converter using the DGD2110

Input resistors

The IC PWM inputs, HIN, LIN and SD, are very high impedance inputs with pull down resistors to VSS for all inputs (see Figure 2); the pull-down resistors have an approximate value of 750kΩ.

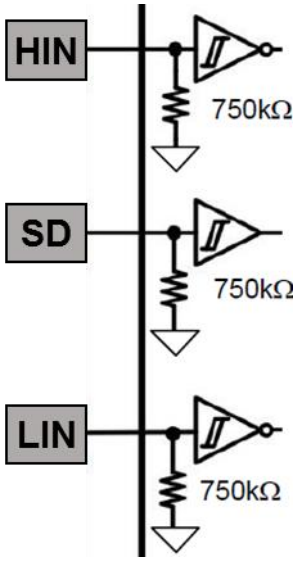

Figure 2. Input logic for the DGD2110/2113

Minimum Pulse Recommendation

The DGD2110/2113 has an RC filter on the input lines to be more resilient in noisy environments. With a rising edge at the input to the gate driver, and then after the propagation delay of the IC, delay from gate resistor, and rise time of the MOSFET, the Half-Bridge will turn on producing bus voltage at the output. This MOSFET turn on produces significant system noise. For optimal operation, it is suggested to provide a minimum pulse width at the input to the IC from the MCU to ensure the turn off occurs after this event. As a rule of thumb, this minimum pulse should be 2 x propagation delay for high-side/low-side drivers; hence for the DGD2110/2113, it is required to have a minimum pulse of 200ns at the logic inputs. It is important to keep this in mind during turn-on or turn-off of motor or power supply; sometimes duty cycle is allowed to gradually decrease to very small pulse widths, this scheme could violate the above minimum pulse requirement.

The DGD2110/2113 will respond to an input pulse greater than 50ns (approximate value from the RC input filter response) and for an input pulse less than 50ns, there will be no response from the IC.

Bootstrap Component Selection

Bootstrap Resistor

Considering Figure 1, when the Low-Side MOSFET (Q2 or Q4) turns on, V_S pulls to GND and the bootstrap capacitor (C_{B1}, C_{B2}) is charged. When the High-Side MOSFET (Q1 and Q3) is turned on, V_S swings above V_{CC} and the charge on the bootstrap capacitor (C_B) provides current to drive the IC High-Side gate driver. The first charge of C_B from V_{CC} through the bootstrap resistor (R_{B1} and R_{B2}) and bootstrap diode (D_{B1} and D_{B2}) occurs when power is first applied and Low-Side turns on the first time. At this time the charge current is the largest as typically C_B is not discharged fully at each cycle during normal operation.

A bootstrap resistor (R_{BS}) is included in the bootstrap circuit to limit the inrush current that charges C_B when V_S pulls below V_{CC}; this inrush current is largest with the first charge. Limiting inrush current is desirable to limit noise spikes on V_S and COM, potentially causing shoot-through. The amplitude and length of time of the inrush current is determined mostly by the component value of R_{BS} and C_{BS} as well as V_{CC} level. The aim in resistor selection for the application is to slow down the inrush current but have limited effect on the RC time constant of charging C_{BS}.

Typically, values for R_{BS} are 3Ω to 10Ω, enough to dampen the inrush current but have little effect on the V_{BS} turn on. Below are some waveforms illustrating the effect of different R_{BS} values.

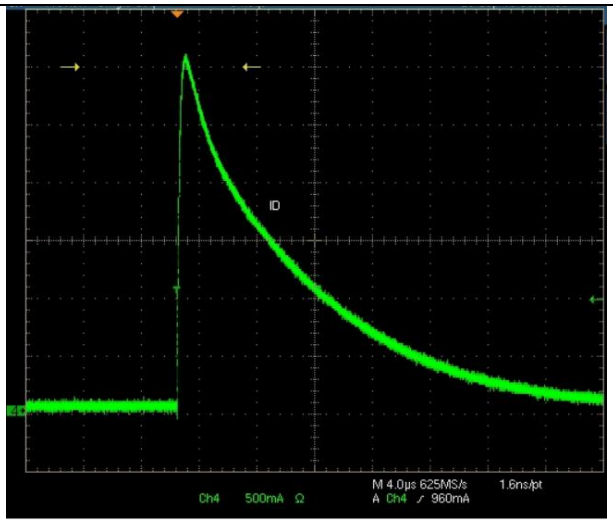

Figure 3. Bootstrap inrush current with R_{BS}=3Ω, C_{BS}=2.2µF

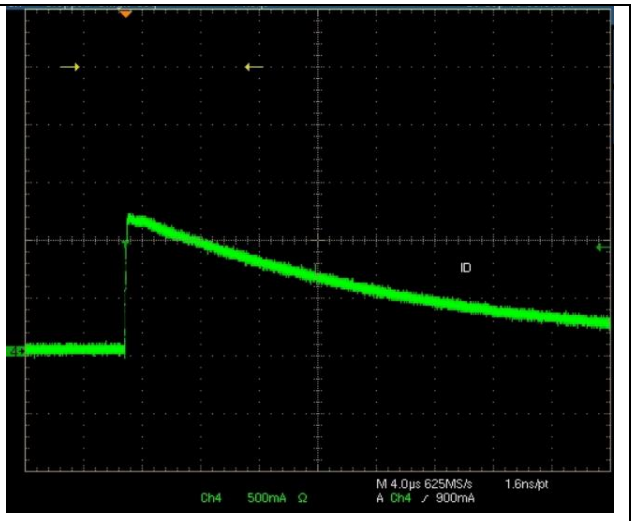

Figure 4. Bootstrap inrush current with R_{BS}=10Ω, C_{BS}=2.2µF

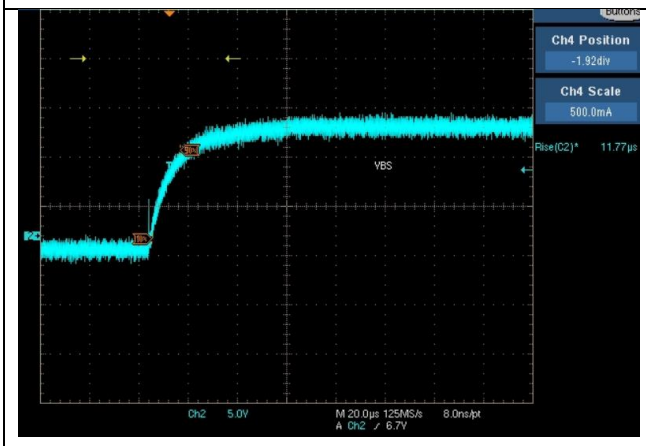

Figure 5. V_{BS} rise time (11.8µs) with C_{BS}=2.2µF and R_{BS}=3Ω resistor

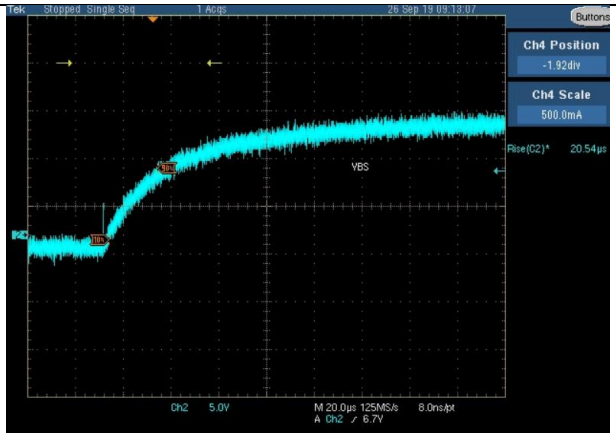

Figure 6. V_{BS} rise time (20.5µs) with C_{BS}=2.2µF and R_{BS}=10Ω resistor

Bootstrap Diode

The chosen bootstrap diode (D_{BS}) should be rated higher than the maximum rail voltage since the diode must be able to block the full rail voltage and any spikes seen at the V_S node. The diode's current rating is simply the product of total charge (Q_T) required by the HVIC and the switching frequency. An ultrafast recovery diode is recommended to minimize any delay of charging the C_{BS} cap. A 1A ultrafast recovery diode is typical for DGD2110/2113 applications.

Bootstrap Capacitor

The initial step in determining the value of the bootstrap capacitor is to determine the minimum voltage drop (ΔV_{BS}) that can be guaranteed when the high-side device is turned on. In other words, the minimum gate-source voltage (V_{GSmin}) must be greater than the UVLO of the High-Side circuit, specifically V_{BSUV-} level. Therefore, if V_{GSmin} is the minimum gate-source voltage such that

$V_{GSmin} > V_{BSUV-}$

Then:
$\Delta V_{BS} = V_{CC} - V_F - V_{GSmin} - V_X$

Where

- V_{CC} is the supply voltage to the DGD2110
- V_F is the voltage drop across the bootstrap diode (D_{BS})
- V_X is the voltage drop across the MOSFET

For an IGBT, V_X is V_{CE-ON} of the IGBT at the specified output current; for a MOSFET it is calculated as the current seen across MOSFET multiplied by its $R_{DS(ON)}$.

In addition to the voltage drops across these components, other factors that cause V_{BS} to drop are leakages, charge required to turn on the power devices, and duration of the High-Side on time. The total charge (Q_T) required by the gate driver then equals:

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}] * T_{HON}$

Where

Q_G = gate charge of power device
Q_{LS} = level shift charge required per cycle
T_{HON} = high-side on time
I_{LK_N} = sum of all leakages that include:

- I_{GSS}/I_{GES}: Gate-source leakage of the power device
- I_{LK_DB}: Bootstrap diode leakage
- I_{LK_IC}: Offset supply leakage of HVIC
- I_{QBS}: Quiescent current for high-side supply
- I_{LK_CB}: Bootstrap capacitor leakage

Bootstrap capacitor leakage (I_{LK_CB}) only applies to electrolytic types. Therefore, it is best not to use electrolytic capacitor. Thus, bootstrap capacitor leakages will not be included in the calculations.

Q_{LS} is not listed in the datasheet; depending on the process technology, it could range anywhere from 3-20nC for 500V to 1200V process respectively. Assuming a value of 10nC for Diodes' 600V process should be sufficient with added margin.

From the basic equation, then the minimum bootstrap capacitor is calculated as:

$CB_{min} \geq Q_T / \Delta V_{BS}$

Example using IGBT
The follow example uses an IGBT as the switching device with the following and desired parameters:

- Power device = DGTD65T15H2TF
- HVIC gate driver = DGD2110
- V_{CC} = 15V
- Q_G = 61nC
- I_{GSS} = 100nA
- T_{HON} = 30µS
- V_{CE} = 1.5V
- I_{OUT} = 5A
- I_{QBS} = 230µA
- I_{LK_IC} = 50µA
- Q_{LS} = 10nC
- V_F = 1.0V
- I_{LK_DB} = 100µA
- V_{GSmin} = 10V

From equations above:

ΔV_{BS} = 15V- 1.0V-10V-1.5V = 2.5V

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}]*T_{HON;}$ where $I_{LK\_N} * T_{HON}$ = 11.4nC

Thus Q_T = 61nC + 10nC +11.4nC = 82.4nC

Therefore C_{Bmin} = 82.4nC / 2.5V= 33nF

The bootstrap capacitor calculated in this example is the minimal value required to supply the needed charge. It is recommended that a margin of 2-3 times the calculated value be used, minimally. Utilizing values lower than this could result in overcharging of the bootstrap capacitor especially during $-V_S$ transients. Typically, for power supply applications, C_{BS} = 0.1µF to 2.2µF is used, and for motor driver applications, C_{BS} = 1.0µF to 10.0µF is used; also it is recommended to use low ESR ceramic capacitors as close to the V_B and V_S pin as possible (see PCB layout suggestions section).

Gate Component Selection

The most crucial time in the gate drive is the turn-on and turn-off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

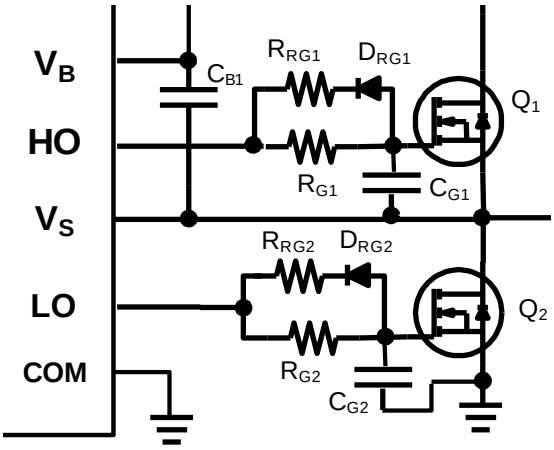

Figure 7. Gate drive high-side and low-side components for DGD2113

Considering the gate driver components for DGD2113 in Figure 7. With the careful selection of R_{G1} and R_{RG1}, it is possible to selectively control the rise time and fall time of the gate drive to the MOSFET. For turn on, all current will go from the IC through R_{G1} and charge the MOSFET gate capacitance, hence increasing or decreasing R_{G1} will increase or decrease rise time in the application. With the addition of D_{RG1}, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitance, through R_{RG1} and D_{RG1} to the driver in the IC to VS for High-Side and COM for Low-Side. So, increasing or decreasing R_{RG1} will increase or decrease the fall time. Sometimes finer control is not needed and only R_{G1} and R_{G2} is used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, and a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. Generally, for power supplies, the switching speed is faster and efficiency is more of a concern, so lower values are recommended, for example R_G = 5Ω - 50Ω. And generally, for motors, the switching speed is slower and the application has more inherent noise, hence higher values are recommended, for example R_G = 20Ω - 100Ω.

To have equal switching times for High-Side and Low-Side, it is recommended that the gate driver components for High-Side and Low-Side are mirrored. For example, R_{RG1}=R_{RG2}, D_{RG1}=D_{GR2} and R_{G1}=R_{G2}.

The gate to source capacitors, C_{G1} and C_{G2}, are used to minimize unexpected shoot through in the Half-Bridge. This shoot through can decrease efficiency or even damage the MOSFETs; this phenomenon is discussed further on page 7.

V_{CC} Decoupling Capacitors

For optimal operation, decoupling is crucial for all gate driver ICs. With poor decoupling, larger V_{CC} transients will occur at the IC when switching, and for greater and longer V_{CC} drop the IC can go into UVLO.

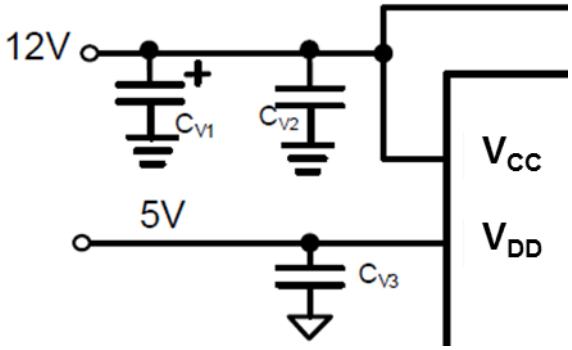

Figure 8. Suggested VCC and VDD decoupling

As shown in Figure 8, two decoupling capacitors (C_{V1} and C_{V2}) are recommended for V_{CC} to power ground and one (C_{V3}) for V_{DD} to logic ground. C_{V1} can be a larger electrolytic, for example 47µF, 50V, used to dampen low frequency drains on supply; C_{V1} does not need to be right next to the IC. But C_{V2} is used to decouple faster edge changes to V_{CC} and should be a low ESR ceramic capacitor placed close to the V_{CC} pin. This component provides stability when V_{CC} is quickly pulled down with load from the IC; typical values are 0.1µF to 1µF. For V_{DD}, switching currents are lower but decoupling is still recommended to minimize noise on logic circuit; typical values are 0.1µF to 1µF close to the device.

For applications with multiple gate driver ICs (for example a full bridge converter as shown in Figure 1), one larger electrolytic (C_{V1}) can be used and the two ceramic caps (C_{V2} and C_{V4}) should be used close to the respective V_{CC} pin (see Layout section also).

High Voltage Decoupling Capacitors

Considering the performance of the whole Half-Bridge, it is important to have appropriate high-voltage decoupling capacitors (see C_{HV1}, C_{HV2}, and C_{HV3} in Figure 1). For best stability (best high-frequency performance), C_{HV2} and C_{HV3} are smaller ceramic capacitors (1µF 450V) placed close to the drain of the MOSFETs at the Half-Bridge (less than 25mm); and then C_{HV1} is the electrolytic bulk capacitor which is typically part of the on board power supply. If the small decoupling capacitors (C_{HV2} and C_{HV3}) are not used, then for optimal operation, the bulk capacitor (C_{HV1}) should be close to the drain of the MOSFETs (less than 25mm).

Separate Logic Ground

In some system designs, to better separate the greater ringing on power ground from logic ground, a separate power ground and logic ground is used. The DGD2110/2113 has a separate logic ground pin (V_{SS}), and internally the logic ground (V_{SS}) and power ground (COM) are separated. The V_{SS} pin is rated to operate from -5V to +5V (where 0V is COM, power ground).

Matching Gate Driver with MOSFET or IGBT

IC drive current and MOSFET/IGBT gate charge

Gate Driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD2110/2113 the drive current is I_{O+} = 2.5A and I_{O-} = 2.5A typical.

For a given MOSFET/IGBT, with the known drive current of the DGD2110/2113, you can estimate how long it will take to turn on/off the MOSFET/IGBT with the equation:

$t = Q_g / I$

Q_g = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current

For example, with the Diodes' DMG10N60SCT, 600V MOSFET, Q_g = 35nC; and with the DGD2110/2113 I_{O+}/I_{O-}, the calculated time is t_r/t_f = 14ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also, an addition of a gate resistor (which is recommended) will increase the t_r and t_f.

Unexpected shoot-through with dV_{DS}/dt

Unwanted MOSFET turn-on, caused by C_{GD} x dV_{DS}/dt (see Figure 9) is often the cause of unexplained shoot through in the Half-Bridge circuit. Depending on the ratio of the C_{GS}/ C_{GD} , when the dV_{DS}/dt across Low-Side MOSFET (Q2) occurs (i.e when High-Side MOSFET turns on), there can be a voltage applied to the gate of the Q_2 MOSFET, turning on Q_2 and causing shoot through. In effect a gate bouncing occurs causing a ringing on the V_S line and the power ground.

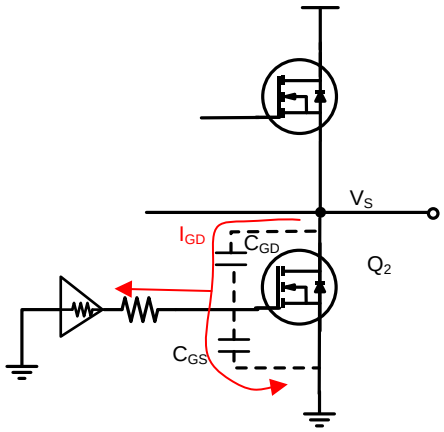

Figure 9. Unexpected shoot through with dV_{DS}/dt

Considering Figure 9:

$I_{GD} = C_{GD}$ x dV_{DS}/dt

I_{GD} will flow towards the resistive load (and small inductance due to parasitics) of the gate driver and the C_{GS} of the MOSFET. Hence this unwanted condition may be minimized by looking at the Ciss/Cres in the MOSFET datasheet (Ciss/Cres gives an indication of C_{GS}/ C_{GD}); having a Ciss/Cres as large as possible will minimize this phenomenon. Also, an external capacitor can be added to the gate-source of the MOSFET (for example 1nF) which will increase C_{GS}/ C_{GD}.

PCB layout suggestions

Layout also plays a considerable role since unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 10 shows the schematic with parasitic inductances in the high current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which would be caused by inductance in the metal of the trace. Considering Figure 10, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible as well as using low ESR ceramic capacitors. Finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

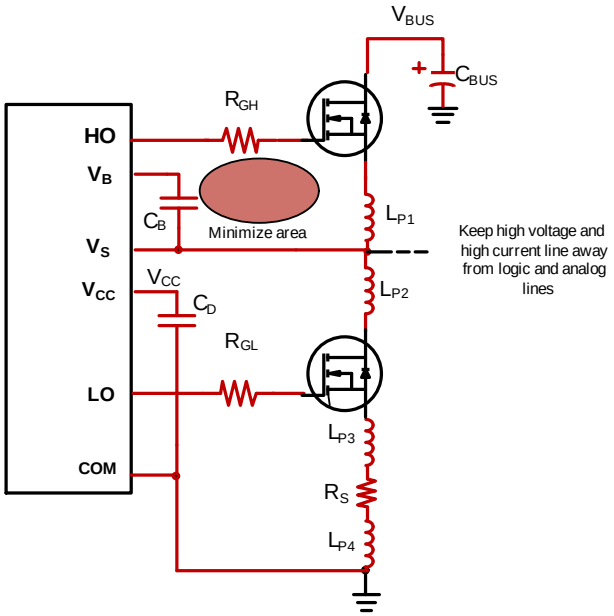

Figure 10. Layout suggestions for DGD2110/2113 in a Half-Bridge, lines in red should be as short as possible

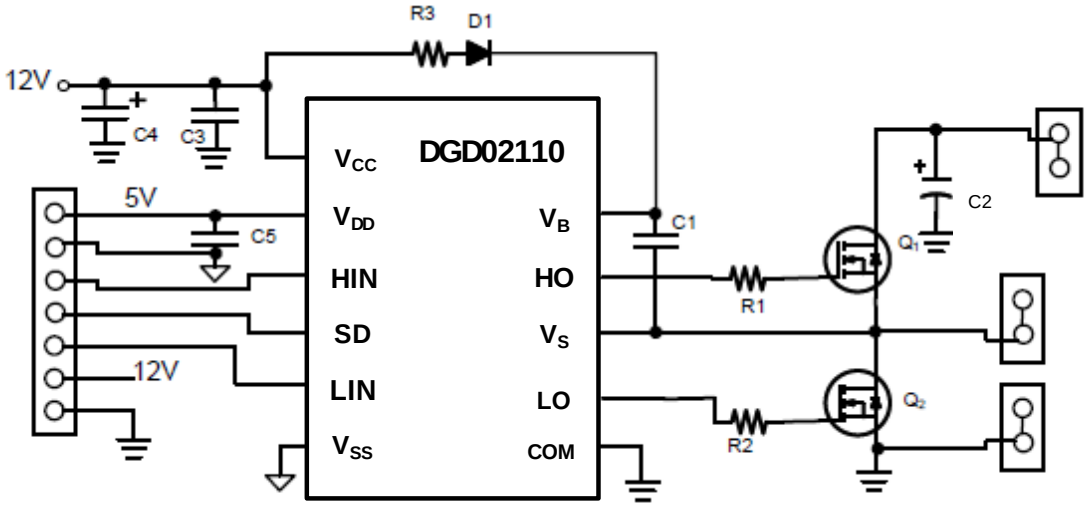

Figure 11. Schematic for layout example shown in Figure 12.

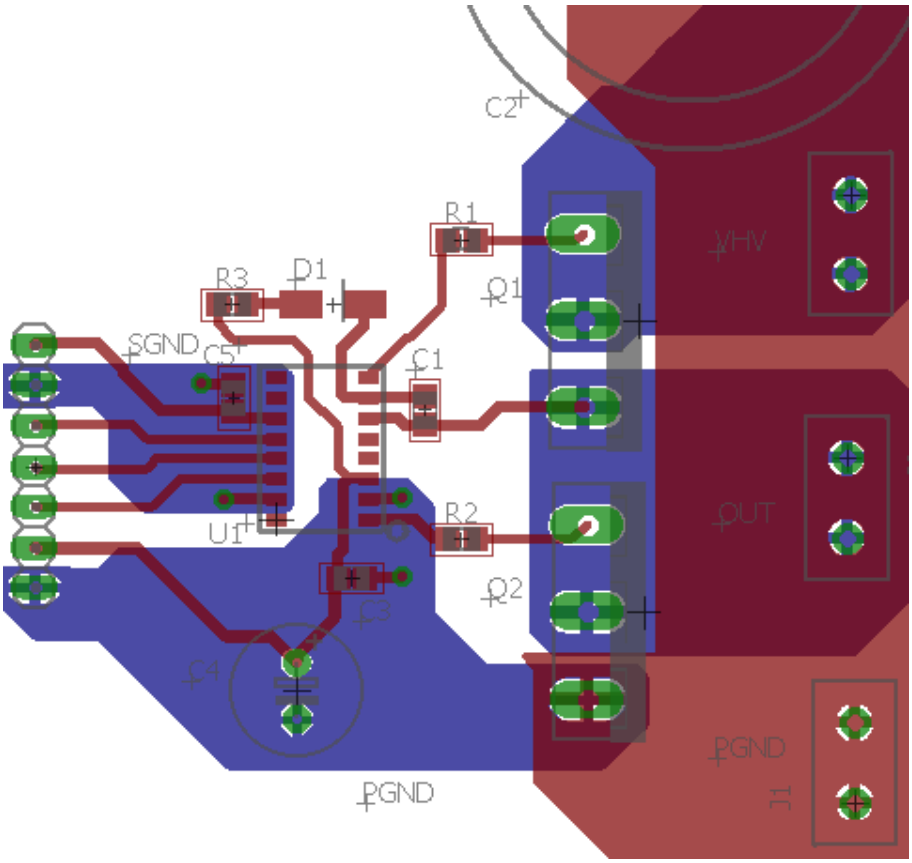

Figure 12. Layout of the schematic shown in Figure 11, DGD2110 in SOIC16, MOSFETs in TO-220, and only bottom of bulk electrolytic (C2) shown

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