AN1184

PI4ULS3V304A / PI4ULS3V504A

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1. Introduction

The PI4ULS3V304A/504A is a four-bit configurable dual-supply autosensing bidirectional level translator that does not require a direction control pin. It can be treated as a four-bit version of PI4ULS3V302/502, but some parameters differ slightly. This device can provide voltage translation between 0.9V and 2.0V (A port) and 1.65V and 3.6V (B port). The speed can be up to 140Mbps (PI4ULS3V304A), or 280Mbps (PI4ULS3V504A) in specific conditions. **The differences between PI4ULS3V304/504 and PI4ULS3V304A/504A are the operating voltages at port A/B, maximum rating and $V_{IHA}/V_{ILA}/V_{IHB}/V_{ILB}$ values. Additionally, the AECQ testing requirement processes are different for PI4ULS3V304/504 and PI4ULS3V304A/504A.**

2. PI4ULS3V304A/504A Mechanism

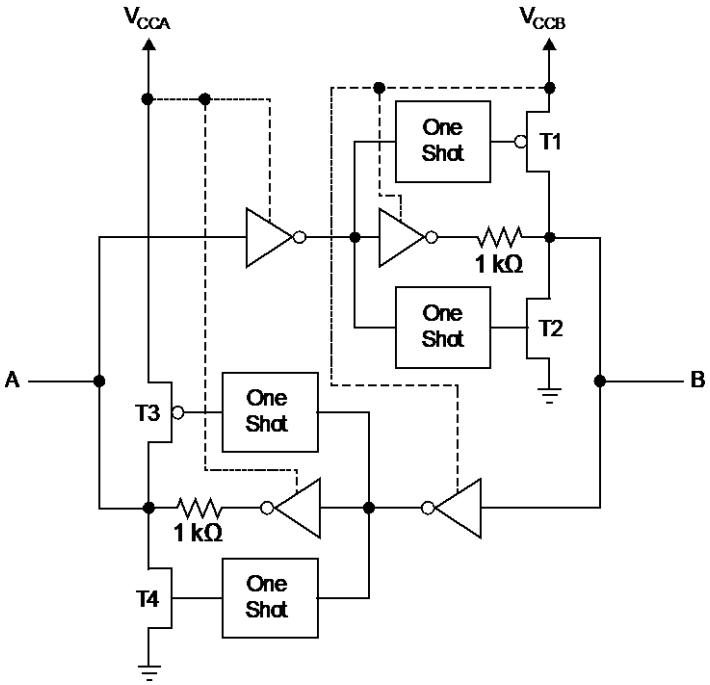

Figure 1. IC block diagram of PI4ULS3V304A/504A

The translator provides bidirectional logic voltage level shifting to transfer data in multiple supply voltage systems. The PI4ULS3V304A/504A does not require a direction control signal to establish the direction of data flow. There is an internal direction-judging block which can provide the direction control. One-shot circuits are used to detect rising or falling input signals. In addition, the one-shot circuits decrease the rise and fall times of the output signal for high-to-low and low-to-high transitions. See Figure 1 for the IC block diagram.

For working diagrams see Figures 2 and 3. The PI4ULS3V304A/504A can detect the rising/falling edge and voltage level at the A/B port. The driver and one-shot circuit at the B port can detect the edge and voltage of the A port, while the driver and one-shot circuit at the A port can detect the edge and voltage of the B port. The weak buffer driver is voltage-level triggered, and the one-shot block is edge triggered.

For example (see Figure 3): ① The external device is driving the A port to a high state, and the voltage level can meet the VIH. ② The weak buffer driver of the B port will pull the B port to high through the 1kΩ resistor. The one-shot circuit of the B port will be active and the T1 PMOS will pull the B port to a high state. ③ When the B port is in a rising edge, the A port detects this behavior, and the one-shot block and buffer driver at the A port pull the A port to a high state through the 1kΩ resistor.

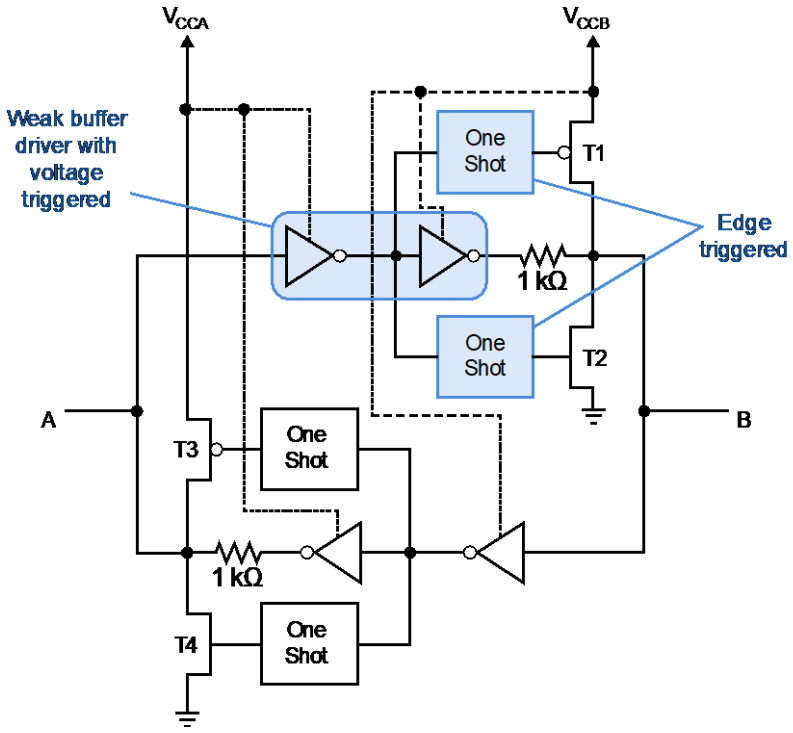

Figure 2. Circuit trigger type of PI4ULS3V304A/PI4ULS3V504A

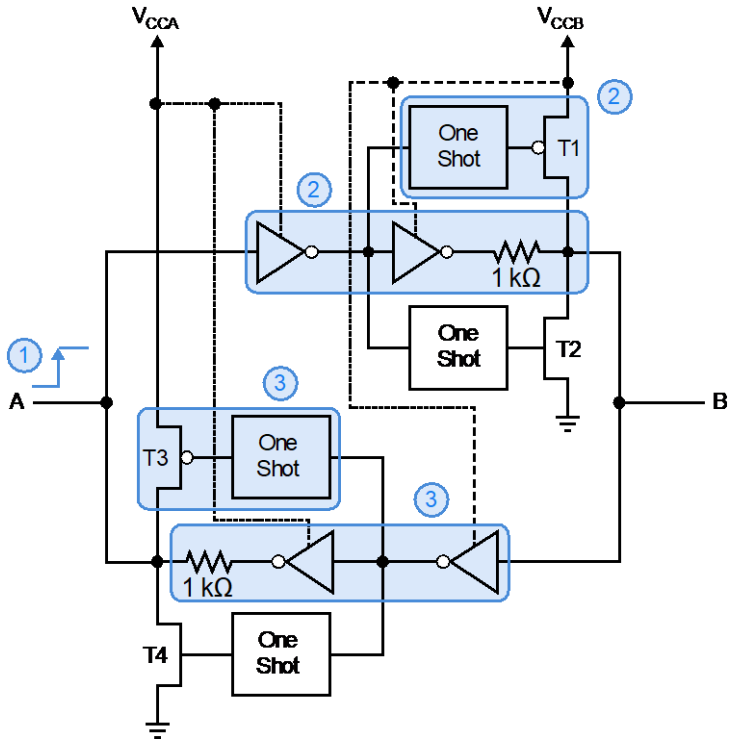

Figure 3. Working diagram of PI4ULS3V304A/PI4ULS3V504A

Furthermore, when one side is an input and other side is an output (e.g., A port as input, B port as output), if the A port input is in a high state, the output buffer on the A port will also drive a high state through a series 1kΩ inside the chip, so the series 1kΩ will be the internal pull-up resistor of the A port. The equivalent circuit is shown in Figure 4.

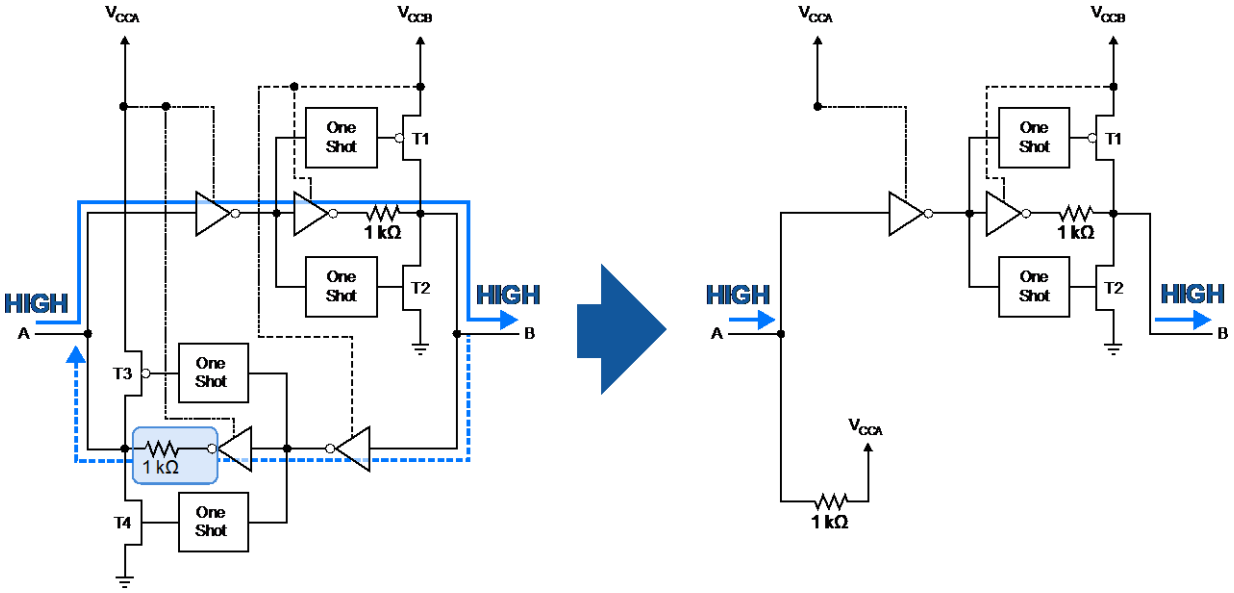

Figure 4. Equivalent circuit of PI4ULS3V304A/504A when drive is high

When one side is an input and other side is an output (e.g., A port as input, B port as output), if the A port input is a low state, the output buffer on the A port will also be driving a low state through a series 1kΩ inside the chip, so the series 1kΩ will be the internal pull-down resistor of the A port. The equivalent circuit is shown in Figure 5. If the action above is changed to the B port as input and the A port as output, all actions will be reversed.

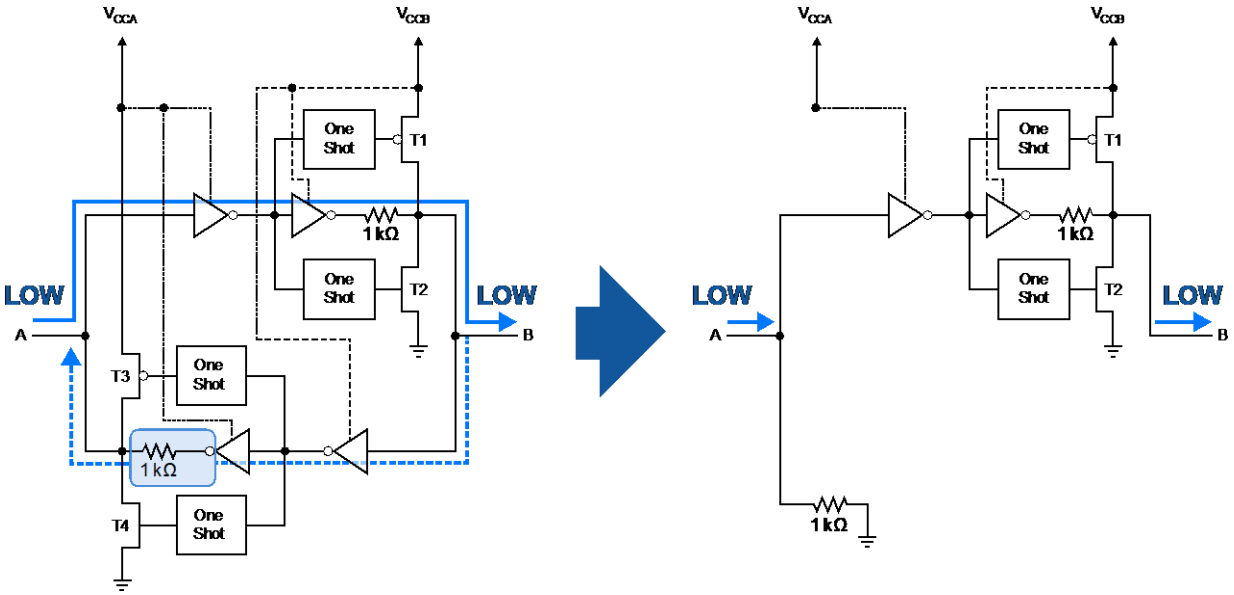

Figure 5. Equivalent circuit of PI4ULS3V304A/504A when drive is low

3. One-Shot Circuits

The translators incorporate a weak buffer with one-shot circuitry to improve switching speeds for rising and falling edges. When the A port is connected to a system driver and driven high, the weak 1kΩ buffer drives the B port high in conjunction with the upper one-shot active. Then the B port is driven high by both the buffer and the T1 PMOS (see Figure 1). The output impedance seen on the B port becomes lower when the one-shot circuit is active. The one-shot time is about 6 to 8ns for PI4ULS3V304A and 3 to 5ns for PI4ULS3V504A.

On the falling edge, the lower one-shot circuit is triggered and the buffer, along with the T2 NMOS (see Figure 1) is active. Table 1 shows the output impedance when the one-shot is active, but these parameters are only guaranteed by design.

Table 1. One-shot impedance with different VCCs

Symbol	Parameter	VCCB (V)	VCCA (V)	Typ.	Unit
ZOB	B port one-shot output impedance	1.8	0.9 to 2.0	37	Ω
		2.5	0.9 to 2.0	20	
		3.6	0.9 to 2.0	15	
ZOA	A port one-shot output impedance	1.8 to 3.3	0.9	52	
		1.8 to 3.3	1.8	17	
		1.8 to 3.3	2.0	15	

4. Input/Output Current and Input/Output-Driven Ability Requirement

The translator has the 1kΩ impedance buffer inside and can be easily overdriven by a system driver connected to the A or B port when a bus direction change is desired.

For example, when the A port is connected to a system driver and driven high, the IIN = VIN/1kΩ when the input voltage is not up to VT (VT is the threshold voltage of PI4ULS3V304A/504A, normally 0.5*VDD). As long as the input voltage is greater than VT, the translator will recognize this to a high level, and drive the B port high. Then the weak buffer in the A port will change from pull-down to pull-up. In this condition the I_{IN} = -(VDD-VT)/1kΩ. For proper operation, the input driver to the translator should be capable of driving 3mA of peak output current.

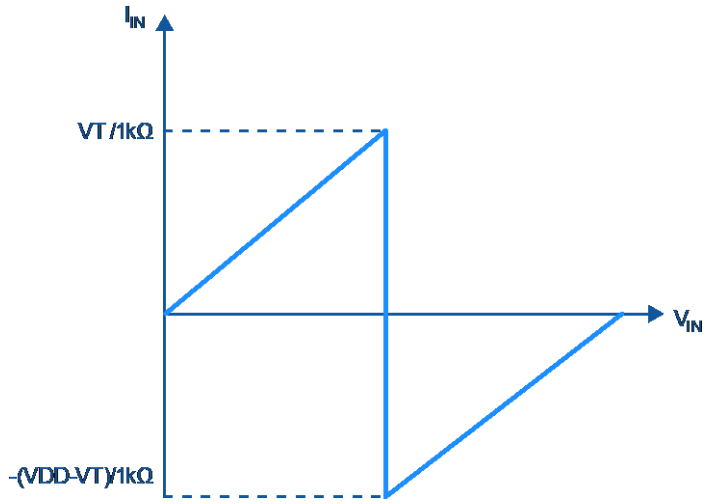

Figure 6. Input current and input-driven ability of PI4ULS3V304A/504A

The IOHA, IOLA, IOHB and IOLB of PI4ULS3V304A/504A will relate to the IIH/IIL and VIH/VIL of the device which connects to PI4ULS3V304A/504A's A or B port. The formula below describe the relationship between IOHA, IOLA, IOHB and IOLB and the device's IIH/IIL/VIH/VIL. **Be aware that this formula does not include the external resistor effect; if the application has an external resistor on PI4ULS3V304A/504A's A/B port then the formula below cannot be used for current-driven ability calculation:**

$$I_{OH(max)} \leq \frac{Vcco - V_{IH(Device)}}{1k\Omega}$$

$$I_{OL(max)} = I_{IL(Device)} = \frac{V_{IL(Device)}}{1k\Omega}$$

According to the formula above, if the IIH(Device) is too strong then the VOH of PI4ULS3V304A/504A will be dropped, which means that the output-driven ability of PI4ULS3V304A/504A depends on the VIH(Device) and the IIL(Device). Figures 7 and 8 show the equivalent circuit of the IOHA, IOLA, IOHB and IOLB calculation.

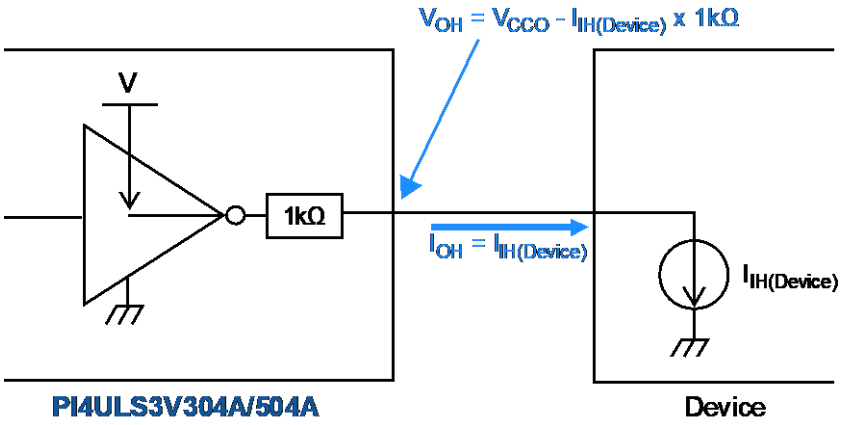

Figure 7. Equivalent circuit when PI4ULS3V304A/504A is driving high to the device

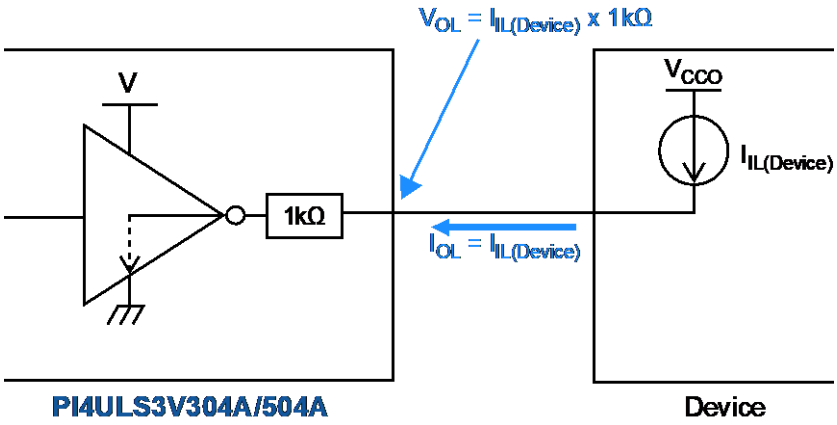

Figure 8. Equivalent circuit when PI4ULS3V304A/504A is driving low to the device

5. External Pull-Up/Pull-Down Resistor

The devices used for driving high impedance loads do not need pull-up or pull-down resistors. But if the application requires an external pull-up or pull-down resistor (PUR or PDR), there is some limitation of the resistor value. When the output is in a steady high or low DC state, it is exclusively driven by the 1kΩ impedance buffer. If an external resistor is added as either a pull-up or pull-down, a resistor divider network will be formed with the 1kΩ buffer. **If the value of the resistor is too small, the V_{OH} or V_{OL} will be adversely impacted. If the value is large (i.e., >50kΩ), there will be very little change in the output voltage level.**

The formula helps to illustrate how an external pull-up resistor affects the output V_{OL} levels. Figures 9 and 10 show the examples of different output levels by pull-up or pull-down resistors. If an external 50kΩ resistor is connected as a pull-up resistor, then:

$$V_{OL} = \frac{1k}{50k + 1k} * Vcco = 0.020 * Vcco$$

$$V_{OH} = 0.9 * Vcco \text{ (min. value, refer to datasheet)}$$

If an external 50kΩ resistor is connected as a pull-down resistor, then:

$$V_{OL} = 0.2V \text{ (max. value, refer to datasheet)}$$

$$V_{OH} = \frac{50k}{50k + 1k} * Vcco = 0.980 * Vcco$$

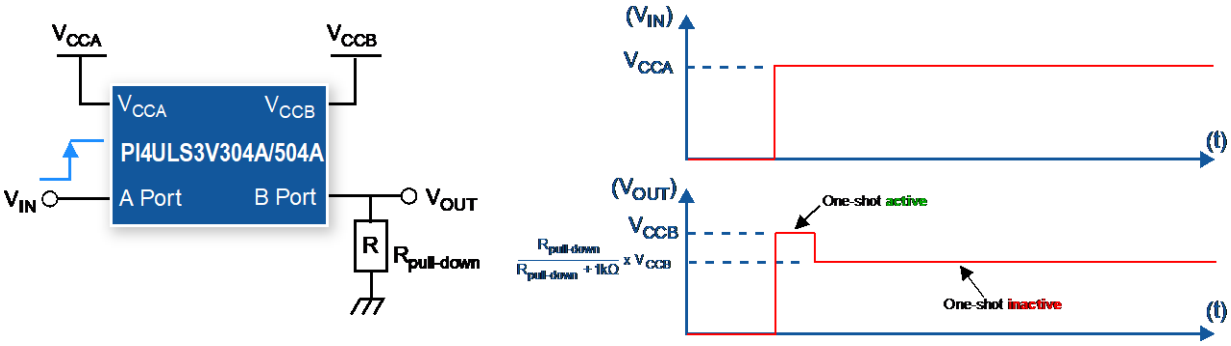

Figure 9. Output voltage with pull-down resistor on the B port

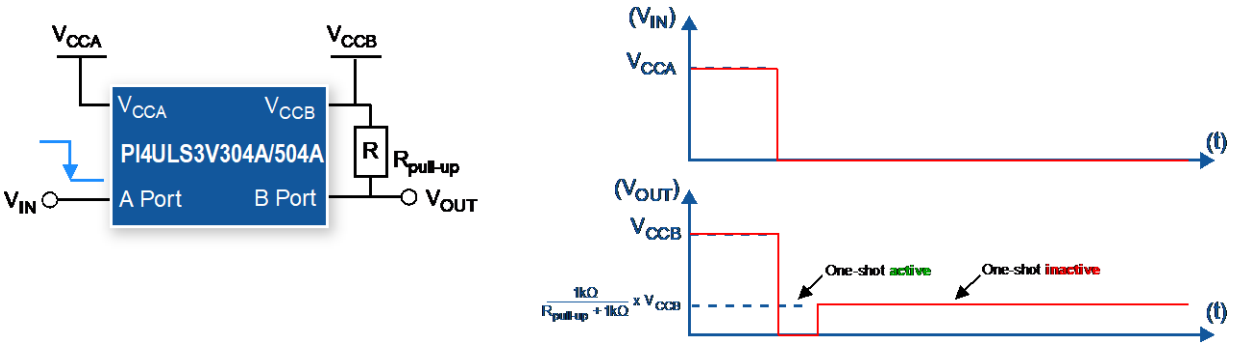

Figure 10. Output voltage with pull-up resistor on the B port

Power-On Pull-Up/Pull-Down I/O state

If the system design must have power-on state high or low (i.e., SPI signal at X86 platform), we recommend referring to the circuit in Figure 11 for design. Because the direction determination of PI4ULS3V304A/504A at the moment of power-on will be affected by different IC corners, due to section 2 mechanism PI4ULS3V304A/504A, I/O unknown (high-Z both sides) when enable is active. **Therefore, we recommend using an RC circuit or CPU control on the EN pin of the PI4ULS3V304A/504A to adjust the enabling time to PI4ULS3V304A/504A, and before enable the CPU out-state must be confirmed by push-pull; the bootstrap stage of the system circuit during power-on is not affected by the initial state of the PI4ULS3V304A/504A.** The RC timing value should follow the minimum requirement of system bootstrap. For suggested timing, see Figures 12a and 12b. **If the RC circuit cannot be used or EN cannot be controlled by CPU in the system, we recommend that the A port and the B port should be ready by push-pull I/O; this is only for the push-pull structure system, not for the open-drain structure system. Do not use open-drain drive source in PI4ULS3V304A/504A**.

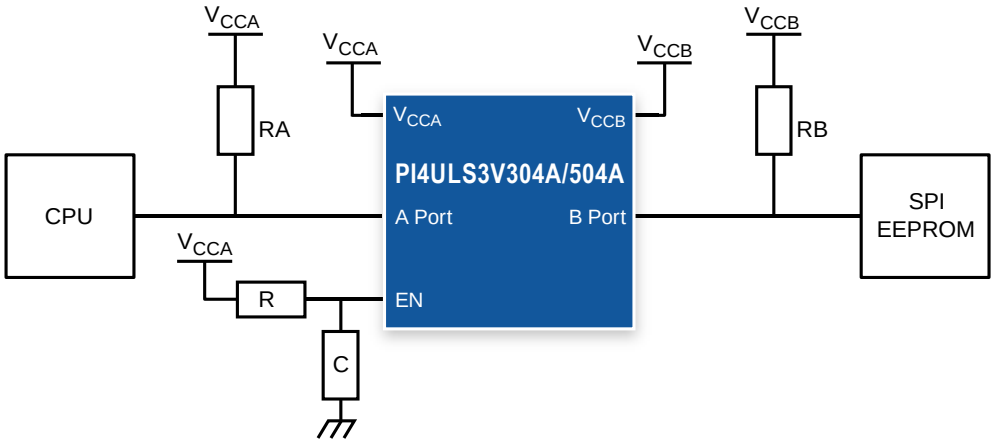

Figure 11. Application circuit for the bootstrap requirement in the system

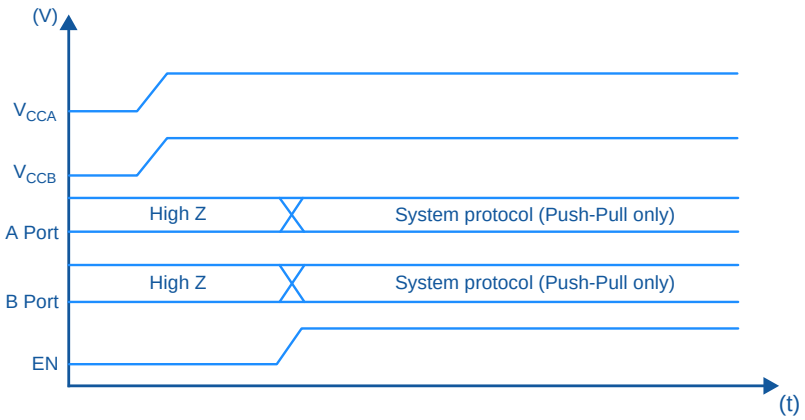

Figure 12a. Timing diagram for the bootstrap requirement in the system (without RA and RB)

Figure 12b shows CPU to 3V304A/504A A port, B port as output, where the B port initial state is high (pull-up 10k) and the A port is non-pull-up, then the B port remains high after enable until the system protocol is active.
If the user wants the A port initial state as H, then it is necessary to control from the B port, reversing the conditions in Figure 12b.

In the EN pin, **if RC is used, it is strongly suggested to increase the value of C and reduce the value of R**.

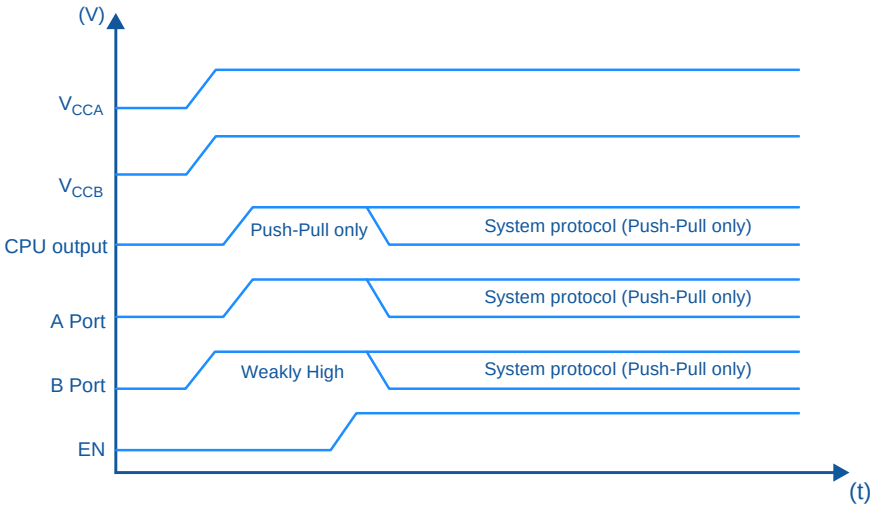

Figure 12b. Timing diagram for the bootstrap requirement in the system (A to B, B initial state H)

6. Recommendation

It is strongly recommended not to use PI4ULS3V304A/PI4ULS3V504A for open-drain applications (i.e., I²C, SMBus), after enable.

7. Capacitance Load and Damping Resistor

The translator will perform better when the load capacitance in the system is smaller. So we suggest setting the capacitance load as low as possible. Of course, the value is determined by the timing requirements and the precise application conditions. But in the worst case, the load capacitance should not be larger than **100pF** when using **PI4ULS3V304A** and should not be larger than **30pF** when using **PI4ULS3V504A**.

When the PI4ULS3V304A/504A operates with a signal greater than 33MHz in system applications (i.e., BIOS SPI on X86 platform), we recommend that a damping resistor (i.e., 33Ω, depending on the system application requirements) be connected in series on the A or B port for better SI quality. For the tested damping resistor and capacitance load combinations, see Tables 2 and 3. **Be aware that the parameters in Table 2 and 3 are for reference only; the actual resistor and capacitance load value still need to be adjusted according to the system application.**

Table 2. PI4ULS3V304A damping resistor and capacitance load combinations

Test condition	Direction	Speed	Series resistor	Capacitive load
VCCA = 1.8V VCCB = 3.3V	A to B	35MHz	33Ω	15pF 30pF 50pF
		70MHz		
	B to A	35MHz		
		70MHz		

Table 3. PI4ULS3V504A damping resistor and capacitance load combinations

Test condition	Direction	Speed	Series resistor	Capacitive load
VCCA = 1.8V VCCB = 3.3V	A to B	70MHz	33Ω	15pF 30pF
		140MHz		
	B to A	70MHz		
		140MHz		

8. Trace Length on PCB

It is suggested that the PCB trace should not be longer than **6 inches** when using **PI4ULS3V304A**, and **4 inches** when using **PI4ULS3V504A**. This is because when the delay time of the trace is longer than the one-shot time, there may be an unexpected status. According to the one-shot structure at the output, a long cable/PCB trace could cause oscillation at the I/O, as shown as Figure 13.

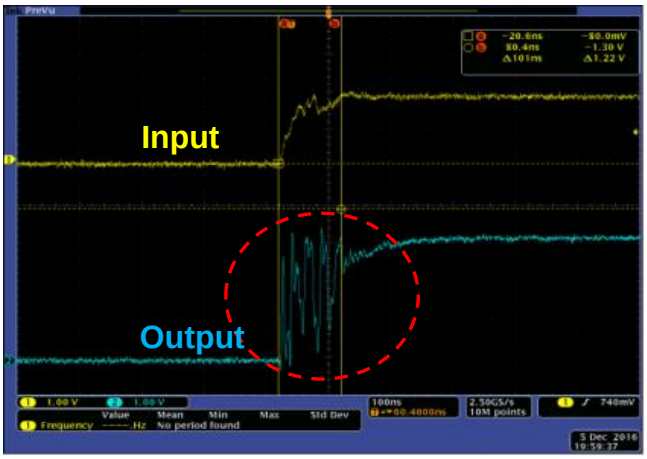

Figure 13. Output oscillating when cable/PCB trace is too long

9. Document Modification History

Version	Description	Author	Date
V01	1. Initial draft.	Kai Xue	05/08/2014
V02	1. Text format adjusted for whole document. 2. Adding the bootstrap condition in Ch.5. 3. Adding VOH formula when output has external pull-up resistor in Ch.5. 4. Adding damping resistor information for >33MHz system application in Ch.6. 5. Adding measurement waveform when cable/PCB trace too long in Ch.7. 6. Adding document modification history in Ch.8.	Carl Che	02/21/2022
V03	1. Modify the chapter title of Ch.5. 2. Modify equations of VOL/VOH in Ch.5. 3. Modify Figure 8 in Ch.5, add signal type when system protocol starts. 4. Adding instructions for one-shot circuit in Ch.3. 5. Fixing typo in Ch.7.	Carl Che	03/09/2022
V04	1. Adding the difference between A version and non-A version IC in Ch.1.	Carl Che	03/16/2022
V05	1. Modify the introduction in Ch.1.	Carl Che	03/23/2022
V06	1. Adding IOH/IOL formula and equivalent circuit in Ch.4. 2. Application definition modified in Ch.5. 3. Adding warning instruction for open-drain applications in Ch.6.	Carl Che	05/05/2022
V07	1. Modify power-on pull-up/pull-down section. 2. Modify Figure 10a and add Figure 10b. 3. Modify Ch.6.	Lance Lan	05/28/2023

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