AN1151

TQFN Package Thermal Pad Via Design Guide

Qin Zhuang, PTC, Diodes Incorporated

1. Introduction

TQFN packages have exposed pads to provide excellent electrical grounding paths to the PCB and transfer the device heat through thermal vias on the PCB thermal landing to the internal copper planes. In order to maximize the removal of heat from the package, the number of vias, the size of the vias, and the construction of the vias must be considered for the thermal landing pattern. The exposed pad must be soldered down to ensure adequate heat conduction from the package. This design guide provides guidelines for the thermal landing pattern design.

2. Thermal Landing Pattern Design

1) The number of thermal vias varies for each product assembled to the PCB. The number of thermal vias depends on the amount of heat that must be moved away from the package and the system work environment, such as ambient temperature, air flow, etc.

   Figure 1 shows the density percentage of the thermal pad via on a four-layer (1oz copper) board vs. the thermal resistance of varying the number of thermal vias (0.33mm diameter). As shown in the Figure 1 curve, too many vias (>22 to 55) will not further improve the thermal transfer through the board. However, too many vias connected to the GND plane will make the PCB assembly soldering difficult because the cold soldering voiding area may be increased on the thermal pad to PCB, which will reduce the thermal resistance efficiency.

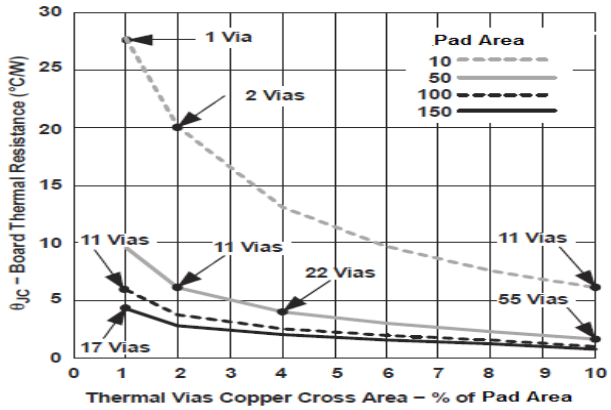


Figure 1. Thermal Resistance per Number of 0.33mm Diameter Vias vs. % of Pad Area

   The general guideline is to make the via pitch 1mm to 1.25mm under the thermal pad. For example, Figure 1 shows that a 5mm × 5mm thermal pad requires $(5 / 1.25)^2 = 16$ vias. The design range is 11 < number of vias < 22.

   For reliability and performance, the die temperature should be limited to a maximum of 125°C. That is, as an estimate, ambient temperature (TA) + device power dissipation × $R_{\theta JA}$ should not exceed 125°C. Therefore depending on device power consumption, the number of vias must be adjusted, such as low P_chip ICs using less vias.

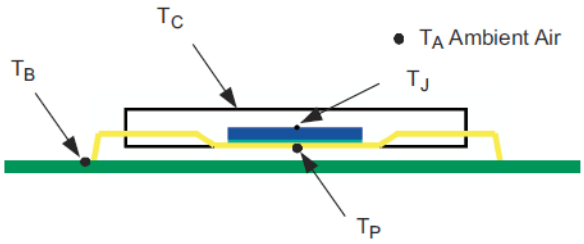
2) The via diameter is typically 0.3mm to 0.33mm for 1oz copper or per PCB manufacturers' guidelines. Larger diameter vias may cause assembly reflow problems.

3) For more PCB layers (>8), thermal vias should be connected to GND planes closer to the component, but these connections should be limited to only one or two but not all GND planes.

4) A PCB assembly can use a conventional plastic package's solder reflow temperature profile (JSTD-020). X-ray inspection must be used to detect voiding within the solder joint. An industrial experiment general guideline recommends a minimum solder joint area of 50% of the package thermal pad area.

3. Appendix

i) Thermal Resistance Diagram



Thermal Resistance Diagram

where

- T_A is the ambient temperature
- T_J is the device junction temperature
- T_C is the case temperature
- T_B is the board temperature at lead
- T_P is the exposed pad temperature

Figure 2. Thermal Resistance Diagram

ii) JSTD Classification Reflow Profiles

Classification Reflow Profiles (1)

	Profile Feature	Sn-Pb Eutectic Assembly	Pd-Free Assembly
$T_{S(max)}$ to T_P	Maximum average ramp-up rate	3°C/second	3°C/second
PREHEAT			
$T_{S(min)}$	Minimum temperature	100°C	150°C
$T_{S(max)}$	Maximum temperature	150°C	200°C
$t_{s(min)}$ to $t_{s(max)}$	Preheat time	60 - 120 seconds	60 - 180 seconds
TIME MAINTAINED			
T_L	Temperature	183°C	217°C
t_L	Time	60 - 150 seconds	60 - 150 seconds
T_P	Peak/classification temperature		
	Maximum ramp-down rate	6°C/second	6°C/second
	Maximum time 25°C to peak temperature	6 minutes	8 minutesThis

(1) All temperatures refer to the topside of the package, measured on the package body surface.