DESCRIPTION

The AP62300T is a 3A, synchronous buck converter with a wide input voltage range of 4.2V to 18V. The device fully integrates a 75mΩ high-side power MOSFET and a 45mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP62300T device is easily used by minimizing the external component count due to its adoption of Constant On-Time (COT) control to achieve fast transient response, easy loop stabilization, and low output voltage ripple.

The AP62300T design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching.

AP62300T is available in a TSOT26 package.

FEATURES

- V_{IN} Range: 4.2V -18V
- Output Voltage range: 0.8V to 7V
- 3A Continuous Output Current
- 0.763V ± 1% Reference Voltage (T_A = +25°C) => AP62300T
- 155µA Low Quiescent Current
- 750kHz Switching Frequency
- Up to 83% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Cycle-by-Cycle Valley Current Limit
  - Thermal Shutdown
- Totally Lead-Free & Fully RoHS Compliant
- Halogen and Antimony Free. “Green” Device

APPLICATIONS

- Flat Screen TV Sets and Monitors
- Consumer Electronics
- Network Systems
- General Purpose Point of Load

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +20.0 (DC)	V
		-0.3 to 22.0 (400ms)	
V_{SW}	Switch Pin Voltage	-1.0 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{EN}	Enable/UVLO Pin Voltage	-0.3 to +6.0	V
V_{FB}	Feedback Pin Voltage	-0.3 to +6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility			
HBM	Human Body Mode	2000	V
CDM	Charge Device Model	500	V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	4.2 to 18	V
V_{OUT}	Output Voltage Range	0.8 to 7	V
T_A	Operating Ambient Temperature	-40 to +85	°C
T_J	Operating Junction Temperature	-40 to +125	°C

SETTING OUTPUT VOLTAGE:

Table 1 for AP62300T shows a list of recommended component selections for common output voltages.

VOUT	C1	C2, C3	R1	R2	L1	C6
1.2V	10µF	2 x 22µF	5.76KΩ	10KΩ	1.5µH	100nF
1.5V	10µF	2 x 22µF	9.76KΩ	10KΩ	1.5µH	100nF
1.8V	10µF	2 x 22µF	13.7KΩ	10KΩ	2.2µH	100nF
2.5V	10µF	2 x 22µF	22.6KΩ	10KΩ	2.2µH	100nF – 220nF
3.3V	10µF	2 x 22µF	33.2KΩ	10KΩ	3.3µH	100nF – 330nF
5.0V	10µF	2 x 22µF	56.2KΩ	10KΩ	3.3µH	100nF – 330nF

Table 1. Common Output Voltages

EVALUATION BOARD

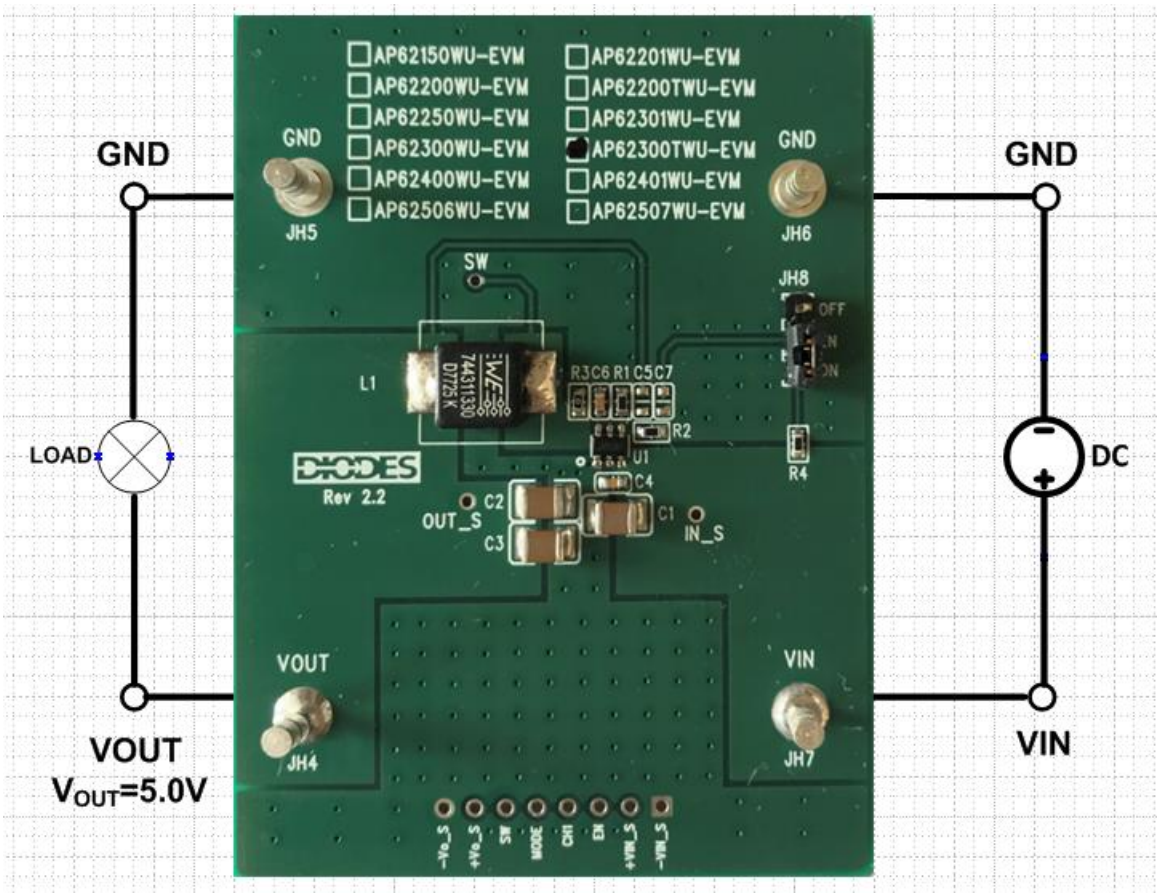


Figure 1. AP62300TWU-EVM

QUICK START GUIDE

The AP62300TWU-EVM has a simple layout and allows access to the appropriate signals through test points. To evaluate the performance of the AP62300TWU, follow the procedure below:

1. Connect a power supply to the input terminals V_{IN} and GND. Set V_{IN} to 12V.
2. Connect the positive terminal of the electronic load to V_{OUT} and negative terminal to GND.
3. For Enable, place a jumper at JH8 to “ON” position to connect EN pin to V_{IN} through 100KΩ resistor to enable IC or leave it OPEN. Jump to “OFF” position to disable IC.
4. The evaluation board should now power up with a 5.0V output voltage.

5. Check for the proper output voltage of 5.0V (±1%) at the output terminals VOUT and GND. Measurement can also be done with a multimeter with the positive and negative leads between VOUT and GND.

6. Set the load to 3A through the electronic load. Check for the stable operation of the SW signal on the oscilloscope. Measure the switching frequency.

MEASUREMENT/PERFORMANCE GUIDELINES:

1) When measuring the output voltage ripple, maintain the shortest possible ground lengths on the oscilloscope probe. Long ground leads can erroneously inject high-frequency noise into the measured ripple.

2) For efficiency measurements, connect an ammeter in series with the input supply to measure the input current. Connect an electronic load to the output for output current.

BOOTSTRAP CAPACITOR GUIDELINES:

To ensure proper operation, a ceramic capacitor must be connected between the BST and SW pins to supply the drive voltage for the high-side power MOSFET. A 100nF ceramic capacitor is sufficient for most applications. In the cases where output voltage is higher than 2.5V, a higher capacitance is recommended to help maintain stable voltage from BST to SW. Please refer to Table 1 for details.

EVALUATION BOARD SCHEMATIC

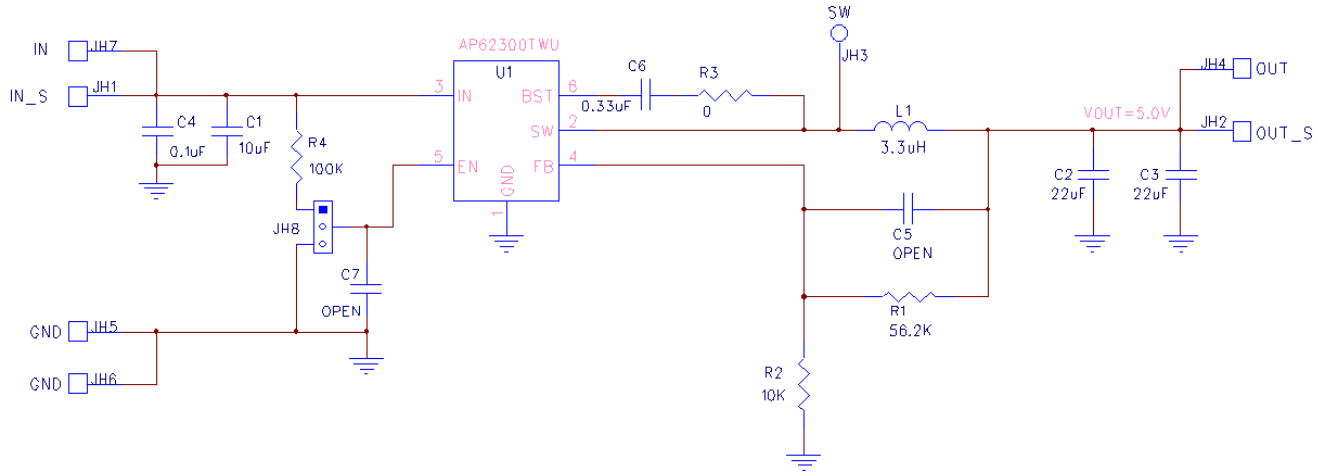


Figure 2. AP62300TWU-EVM Schematic

PCB TOP LAYOUT

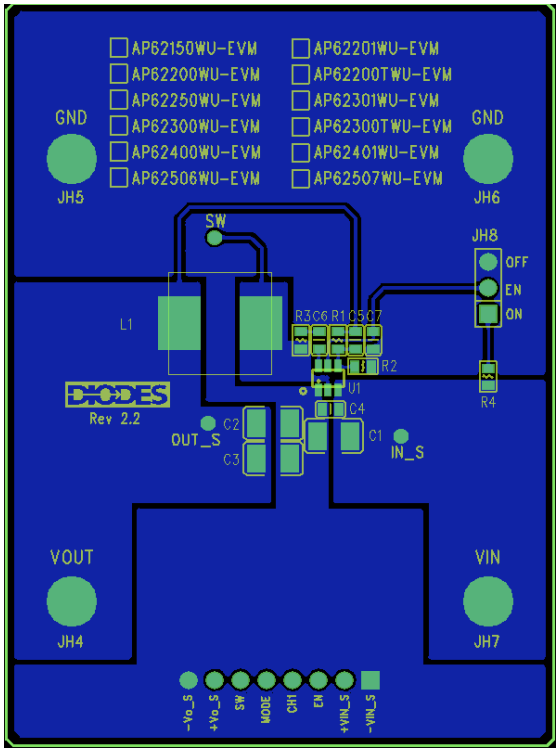


Figure 3. AP62300TWU-EVM – Top Layer

PCB BOTTOM LAYOUT

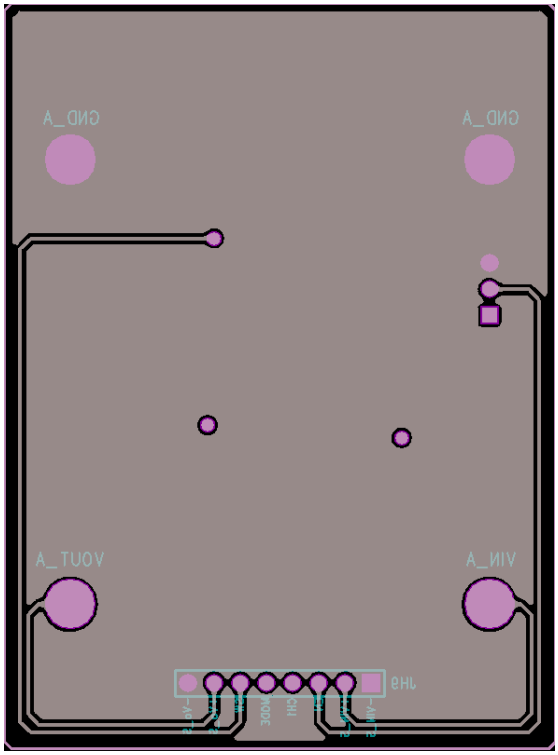
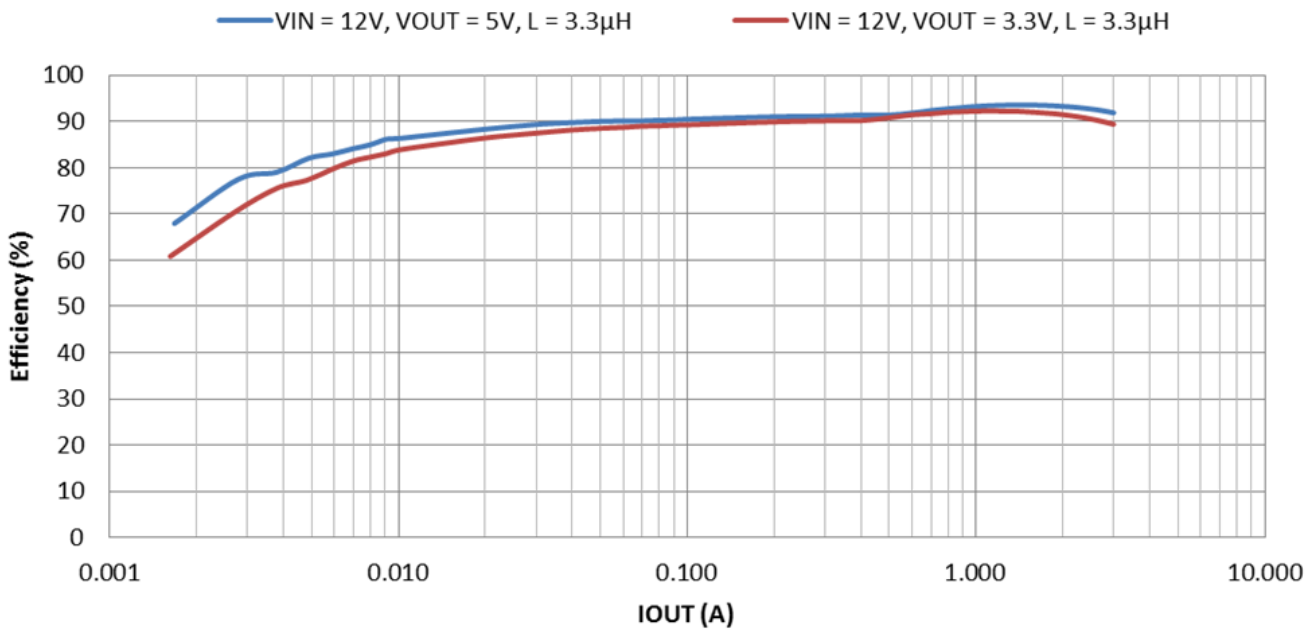


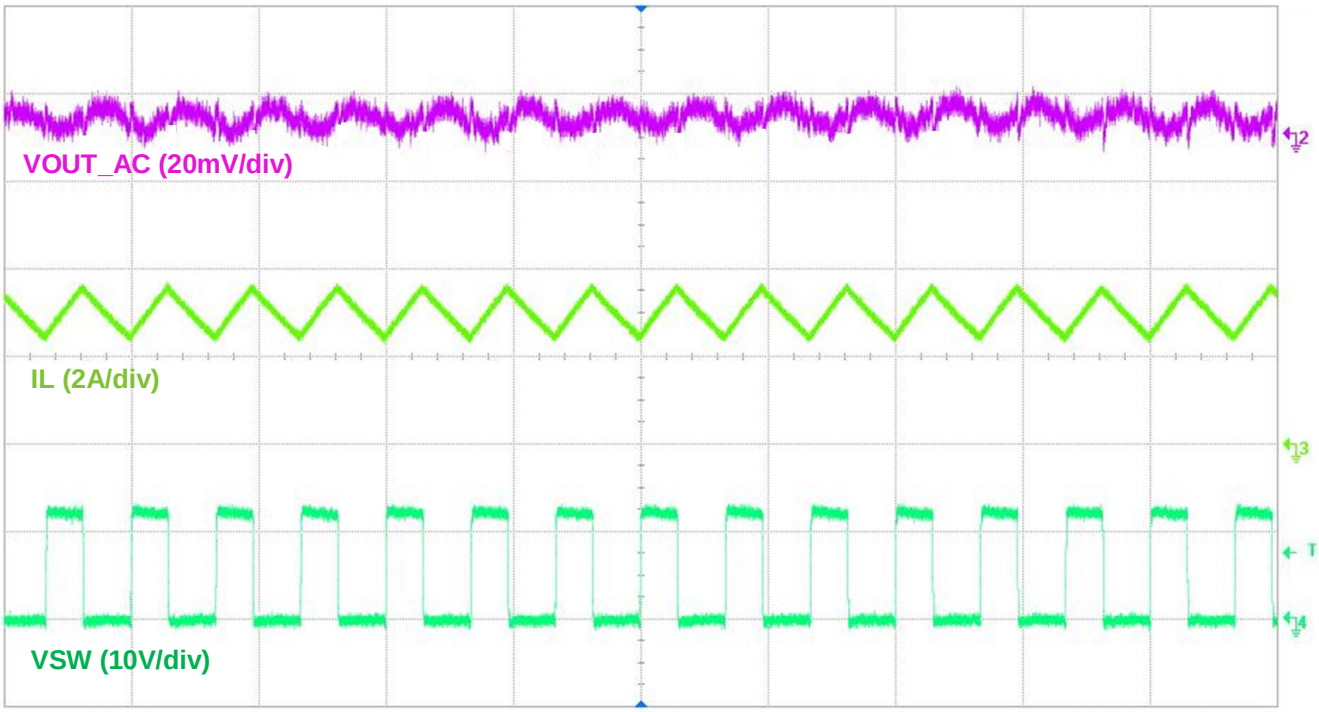
Figure 4. AP62300TWU-EVM – Bottom Layer

BILL OF MATERIALS for AP62300TWU-EVM for V_{OUT}=5V

Ref	Value	Description	Qty	Size	Vendor Name	Manufacturer PN
C1	10µF	Ceramic Capacitor, 25V, X5R	1	1210	Murata	GRM32DR61E106KA12L
C2, C3	22µF	Ceramic Capacitor, 25V, X5R	2	1210	AVX	12103D226KAT2A
C4	0.1µF	Ceramic Capacitor, 50V, X7R, 10%	1	0603	Murata	GCJ188R71H104KA12D
C6	0.33µF	Ceramic Capacitor, 16V, X7R, 10%	1	0603	Samsung	CL10B334KO8NNNC
L1	3.3µH	DCR=10.5mΩ, Ir=7.5A	1	10x10x 5mm	Wurth Electronics	7447714033
R1	56.2KΩ	SMD Resistor, 1%	1	0603	Panasonic	ERJ-3EKF5622V
R2	10KΩ	SMD Resistor, 1%	1	0603	Panasonic	ERJ-3EKF1002V
R3	0Ω	SMD Resistor, 1%	1	0603	Panasonic	ERJ-3GEY0R00V
R4	100KΩ	SMD Resistor, 1%	1	0603	Panasonic	ERJ-3EKF1003V
JH4, JH5, JH6, JH7	1598	Terminal Turret Triple 0.094" L (Test Points)	4	Through-Hole	Keystone Circuit	1598-2
JH8		PCB Header, 40 POS	1	1X3	3M	2340-6111TG
U1	AP62300T	Sync Buck DC-DC converter	1	TSOT26	Diodes Incorporated	AP62300TWU-7

TYPICAL PERFORMANCE CHARACTERISTICS





UVP OPERATION:

UVP is known as Undervoltage Protection. It is a comparator that monitors the output voltage. UVP is intended to assist the OCP (overcurrent protection). In the event that the output is overloaded, then its voltage will drop. At the point when VFB is 495mV, then the LS FET will discharge the output and the regulator will enter hiccup mode to reduce power dissipation. Likewise, the UVP will occur to prevent damage if the output is shorted to ground.

RECOMMENDATION OF ACHIEVING HIGH VIN UVLO THRESHOLD VOLTAGE

For output voltage >4V, it is best to add a resistor at R5 of EN equal to 25KΩ in the resistive divider network so that the turn-off voltage occurs at 4.8V while turn-on voltage occurs at 5.9V. Please refer to the schematic below for higher VIN UVLO threshold in details.

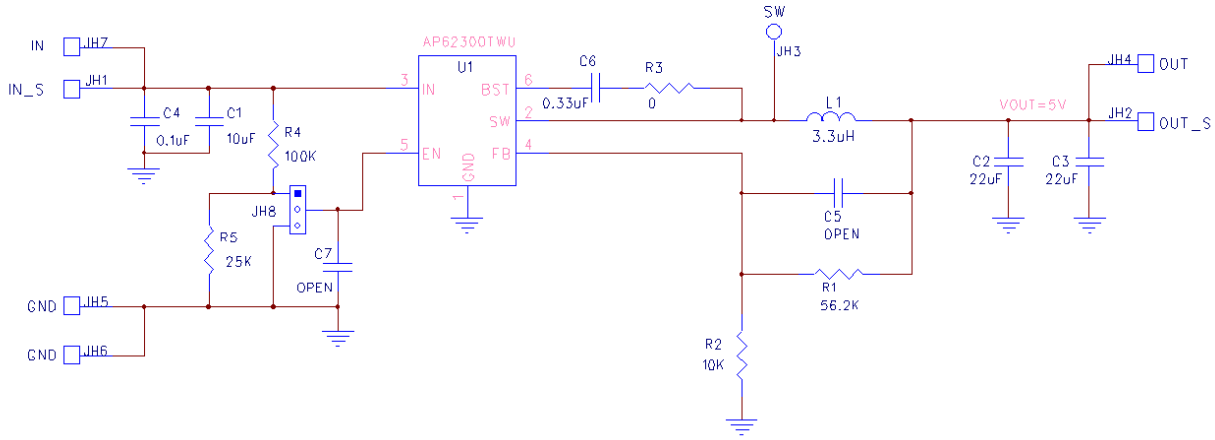


Figure 5. AP62300TWU-EVM Schematic for higher VIN UVLO

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