Description

The AP63300Q is 3A, synchronous buck converter with a wide input voltage range of 3.8V to 32V. The device fully integrates a 75mΩ high-side power MOSFET and a 40mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP63300Q device is easily used by minimizing the external component count due to its adoption of peak current mode control along with its integrated loop compensation network.

The AP63300Q design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching. AP63300Q also features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The device is available in a TSOT26 package.

Features

- VIN 3.8V to 32V
- 3A Continuous Output Current
- 0.8V ± 1% Reference Voltage
- 22µA Ultralow Quiescent Current (Pulse Frequency Modulation)
- 500kHz Switching Frequency
- Supports Pulse Frequency Modulation (PFM)
  - Up to 88% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
- Low-Dropout (LDO) Mode
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection (OVP)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown

APPLICATIONS

- 5V, 12V, and 24V Distributed Power Bus Supplies
- FPGA, DSP, and ASIC Supplies
- Flat Screen TV Sets and Monitors
- White Goods and Small Home Appliances
- Home Audio
- Network Systems
- Consumer Electronics
- Cordless Power Tools
- Optical Communication and Networking Systems
- General Purpose Point of Load

FUNCTIONAL BLOCK

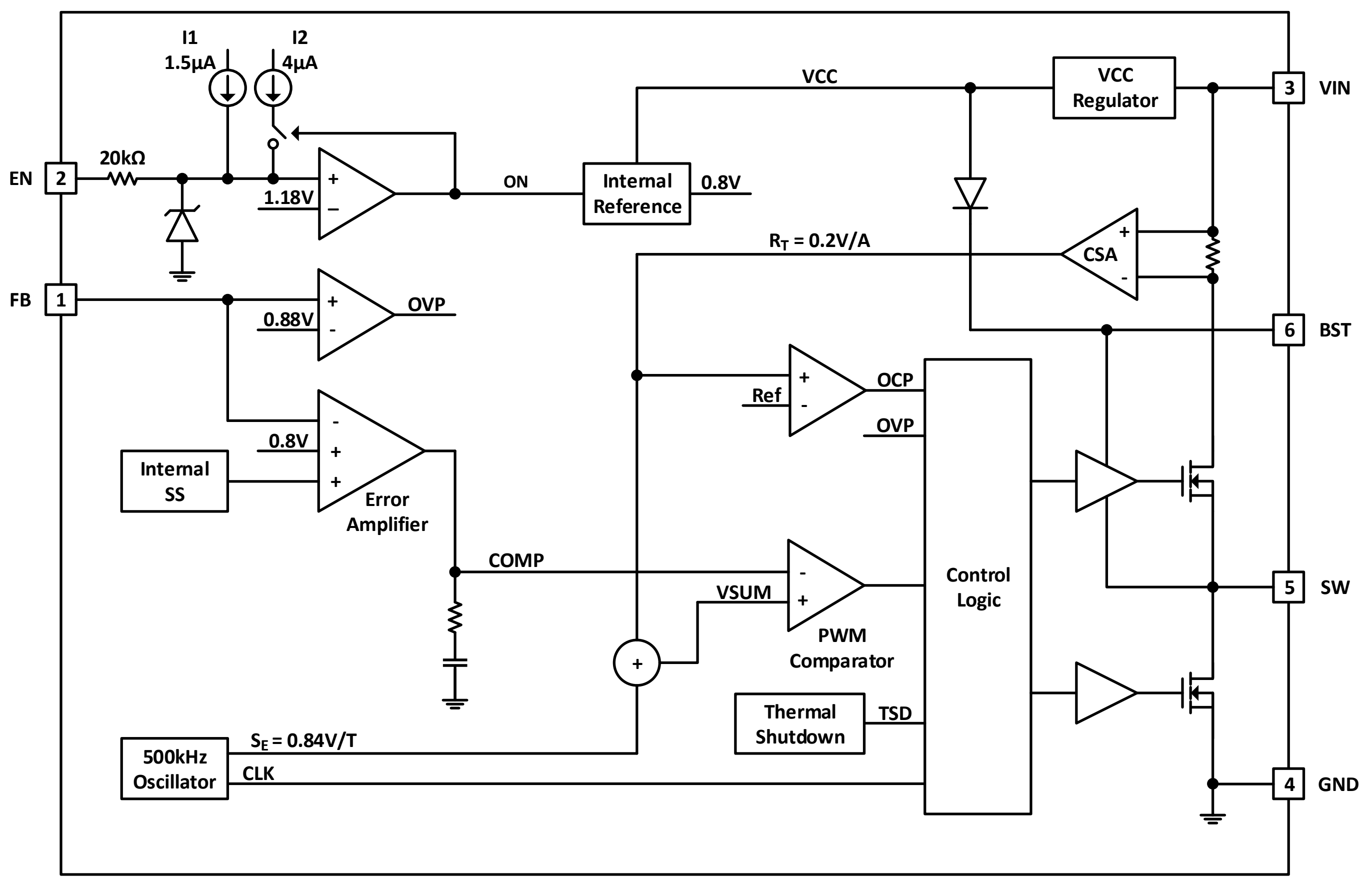

Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +35.0 (DC)	V
		-0.3 to +40.0 (400ms)	
VFB	Feedback Voltage	-0.3V to +6.0	V
VEN	Enable/UVLO Pin Voltage	-0.3 to +35.0	V
VSW	Switch Node Voltage	-0.3 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	V
VBST	Bootstrap Pin Voltage	VSW - 0.3 to VSW + 6.0	V
TST	Storage Temperature	-65 to +150	°C
TJ	Junction Temperature	+160	°C
TL	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Mode	2000	V
CDM	Charged Device Model	1000	V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	3.8	32	V
VOUT	Output Voltage	0.8	31	V
TA	Operating Ambient Temperature Range	-40	+125	°C
TJ	Operating Junction Temperature Range	-40	+150	°C

EVALUATION BOARD

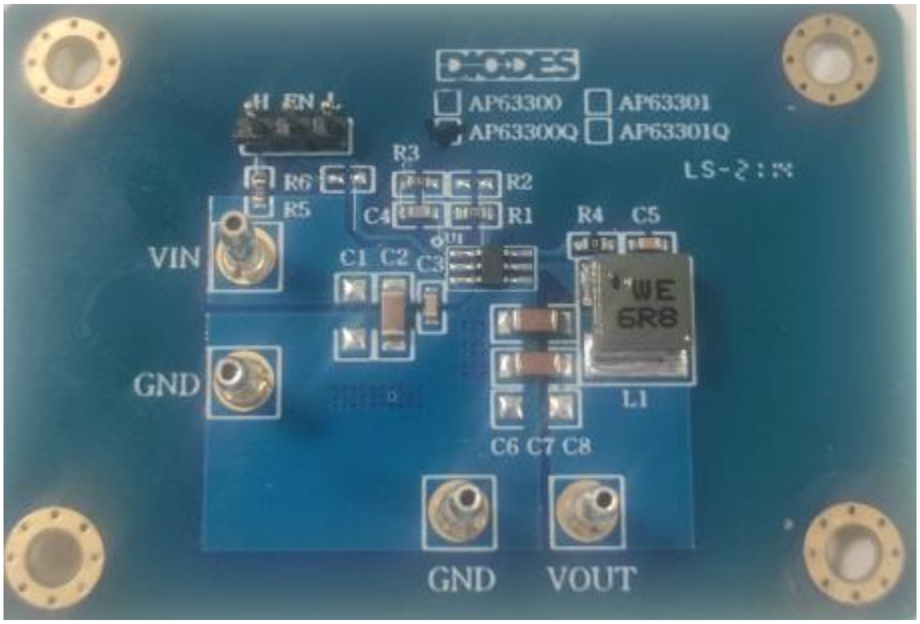

Figure 2. Top Picture of AP63300QWU-EVM Board

QUICK START GUIDE

The AP63300QWU-EVM has a simple layout and allows access to the appropriate signals through test points. To evaluate the performance of the AP63300Q, follow the procedure below:

1. For evaluation board configured at V_{OUT}=5V, connect a power supply to the input terminals V_{IN} and GND. Set V_{IN} to 12V.
2. Connect the positive terminal of the electronic load to V_{OUT} and negative terminal to GND.
3. For Enable, place a jumper to “H” position to enable IC. Jump to “L” position to disable IC.
4. The evaluation board should now power up with a 5V output voltage.
5. Check for the proper output voltage of 5V (±1%) at the output terminals V_{OUT} and GND. Measurement can also be done with a multimeter with the positive and negative leads between V_{OUT} and GND.
6. Set the load to 3A through the electronic load. Check for the stable operation of the SW signal on the oscilloscope. Measure the switching frequency.

MEASUREMENT/PERFORMANCE GUIDELINES:

1) When measuring the output voltage ripple, maintain the shortest possible ground lengths on the oscilloscope probe. Long ground leads can erroneously inject high frequency noise into the measured ripple.

2) For efficiency measurements, connect an ammeter in series with the input supply to measure the input current. Connect an electronic load to the output for output current.

Setting the Output Voltage of AP63300Q

1) Setting the output voltage:

   The AP63300Q features external programmable output voltage by using a resistor divider network R3 and R1 as shown in the typical application circuit. The output voltage is calculated as below,

$$V_{OUT} = 0.8 \times \left(\frac{R_1 + R_3}{R_1} \right)$$

   First, select a value for R1 according to the value recommended in the table 1. Then, R3 is determined. The output voltage is given by Table 1 for reference. For accurate output voltage, 1% tolerance is required.

2) Output feed-forward capacitor selection:

   The AP63300Q has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C4 is used to boost the phase margin at the converter cross-over frequency f_C. The feed-forward capacitor is given by Table 1 for reference. The feed-forward capacitor is calculated as below,

$$C_{ff} = \frac{1}{2\pi \times f_C \times R_3}$$

Table 1. Resistor selection for output voltage setting

Vo	R3	R1	C4	C6-C8
1.8V	77.5 KΩ	62 KΩ	100pF	22µFx2
2.5V	131 KΩ	62 KΩ	100pF	22µFx2
3.3V	182 KΩ	62 KΩ	100 pF	22µFx2
5V	157 KΩ	30 KΩ	100 pF	22µFx2
12V	249 KΩ	18 KΩ	56 pF	22µFx4

EXTERNAL COMPONENT SELECTION:

1) Input & output Capacitors (Cin, Cout):
   (1) For lower output ripple, low ESR is required.
   (2) Low leakage current needed, multiple capacitor parallel connection.
   (3) The Cin and Cout capacitances are greater than 10µF and 44µF respective.

2) Bootstrap Voltage Regulator:
   An external 0.1µF ceramic capacitor is required as bootstrap capacitor between BST and SW pins to work as high-side power MOSFET gate driver.

3) Inductor (L):
   (1) Low DCR for good efficiency
   (2) Inductance saturate current must higher than the output current
   (3) The recommended inductance is shown in the table 2 below.

EVALUATION BOARD SCHEMATIC

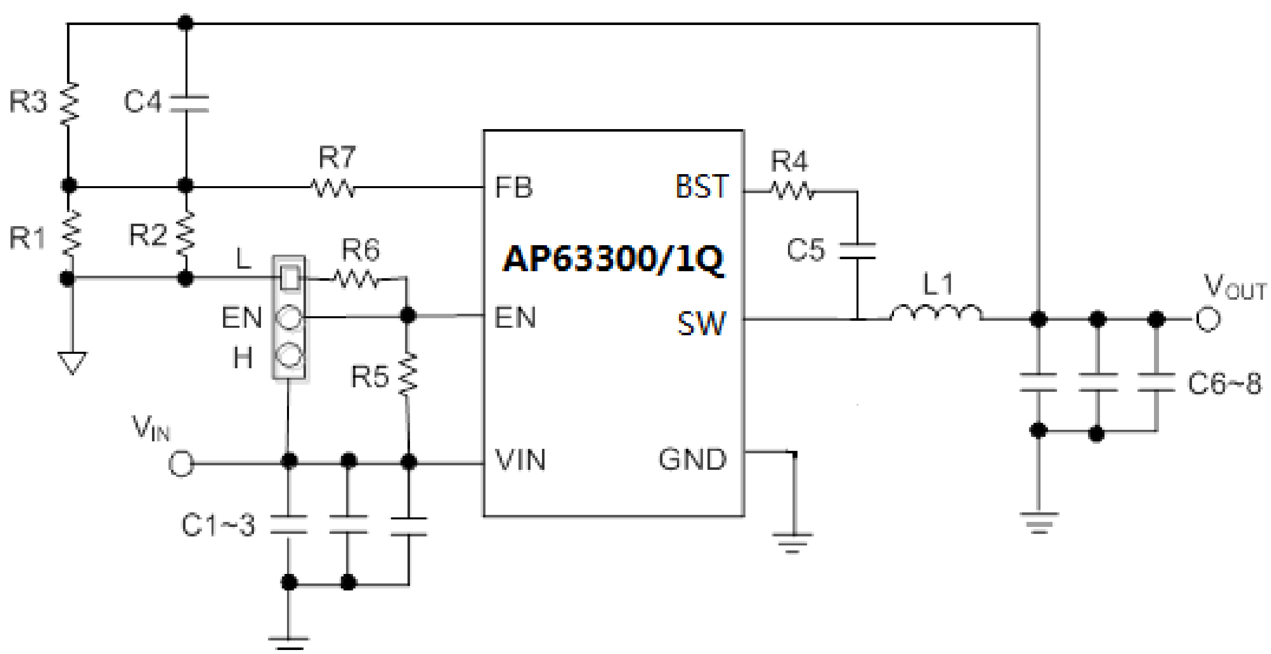

Figure 3. Typical Application Circuit

PCB TOP LAYOUT

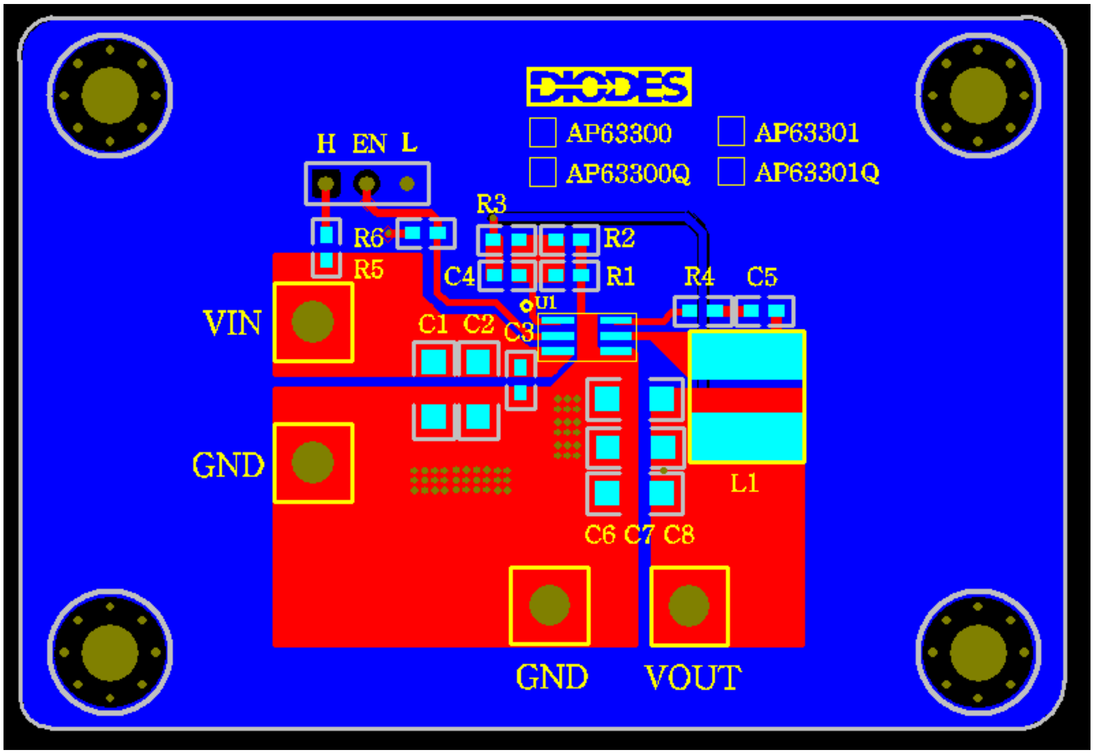

Figure 4. AP63300QWU-EVM – Top Layer

PCB BOTTOM LAYOUT

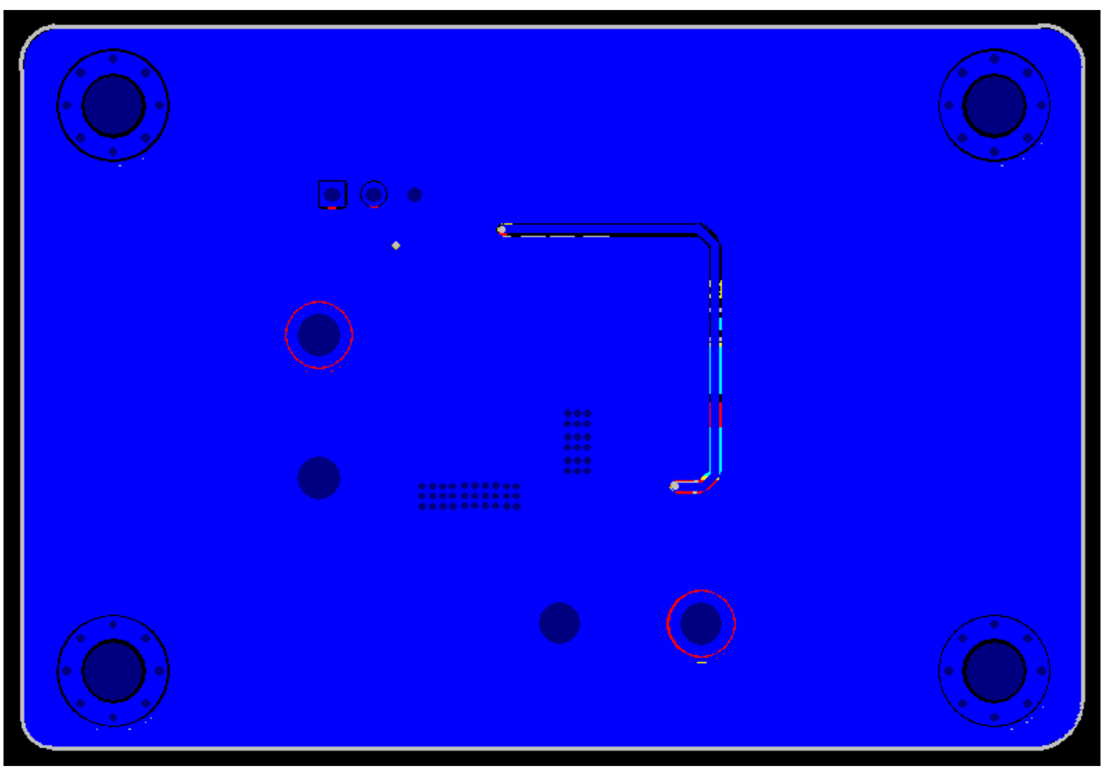

Figure 5. AP63300QWU-EVM – Bottom Layer

BILL OF MATERIALS for AAP63300QWU-EVM

Table 2

Item	Value	Type	Rating	Description	Description
C2	10µF	X7R, Ceramic/1206	35V	Input CAP	TDK CGA5L1X7R1V106K160AC
C3	0.1µF	X8R, Ceramic/0603	50V	Input CAP	TDK CGA3E3X8R1H104K080AB
C4	100pF	C0G, Ceramic/0603	50V	Feedback CAP	TDK CGA3E2C0G1H101J080AA
C5	0.1µF	X8R, Ceramic/0603	50V	Bootstrap CAP	TDK CGA3E3X8R1H104K080AB
C6 & C7	22µF	X7R, Ceramic/1206	10V	Output CAP	TDK CGA5L1X7S1A226M160AC
L1	6.8µH	6060	6.5A	Inductor	Würth PART 744 393 690 68
R1	30K	0603	1%	Voltage set RES*	
R3	162K	0603	1%		
R4	0	0603	1%	Bootstrap RES	
R5	100K	0603	1%	EN pull high RES	
U1		AP63300Q		TSOT23-6	Diodes Incorporated BCD

***Note**: The present value of R3/R1 are based on Vout=5.0V

TYPICAL PERFORMANCE CHARACTERISTICS

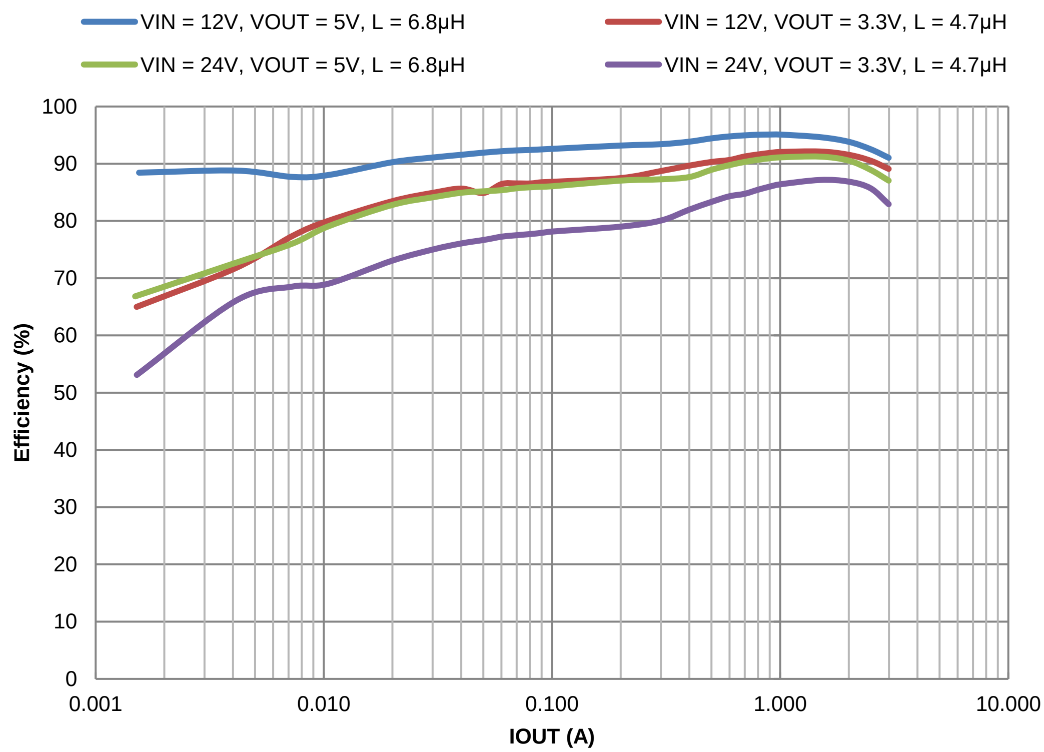

Figure 6. AP63300Q Efficiency vs. Output Current

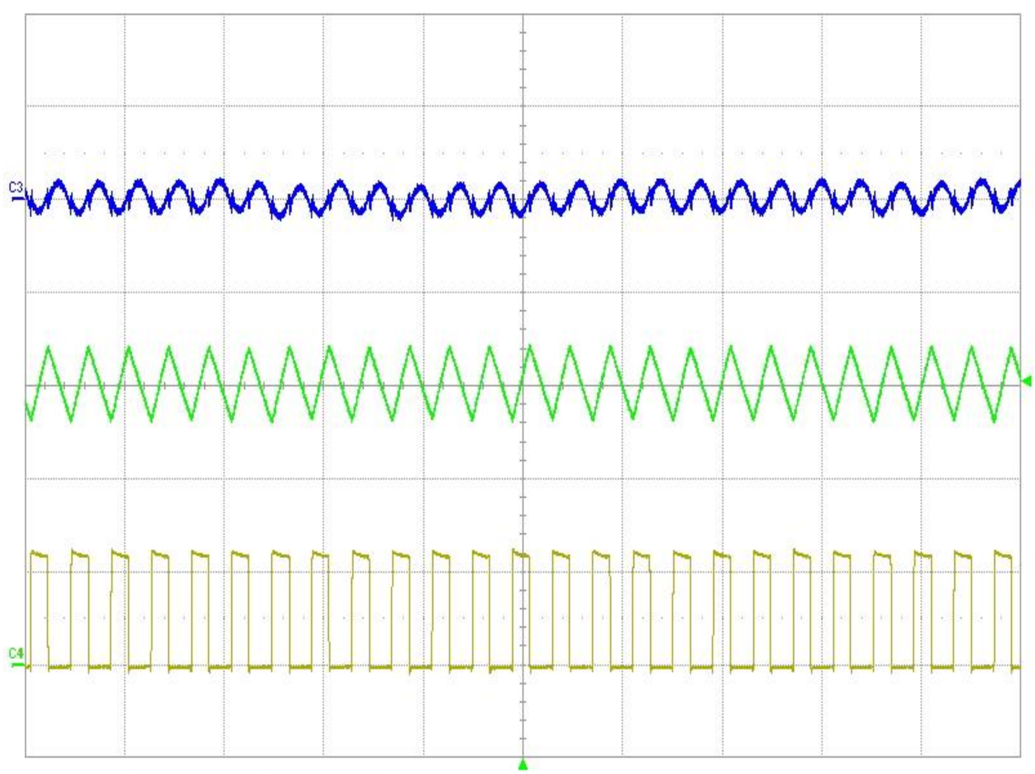

Figure 7. AP63300Q Vin=12V, Vout=5V Output Voltage Ripple, IOUT = 3A