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1 Introduction

PI2EQX862XUAE is a low power, cost effective 8.0Gb/s ReDriver. It can be used to connect a PCIE3.0/SATA3.0 1-lane source to PCIE3.0/SATA3.0 device with M.2, mSATA or SATA Express connectors. PI3EQX862XUAE has one small 18-pin TQFN package with 2x2mm size.

2 External Component Requirements

PI2EQX862XUAE is designed to transmit PCIE3.0 or SATA3.0 signals which are delivered from a source like Intel Skylake PCIE/SATA interface.

2.1 AC Coupling Capacitors on Differential Pairs

In the application, AC coupling capacitors at differential pair signals are inserted at 100nF between host and PI2EQX862XUAE.
Between PI2EQX862XUAE and device, there's no requirement for AC coupling capacitors per SATA/PCIE spec. Generally SATA or PCIE HDD/SSD device will have AC coupling capacitors on it. **But we suggest user to put 220nF capacitors or 0ohm resistors on differential pairs between PI2EQX862XUAE and device connectors.**
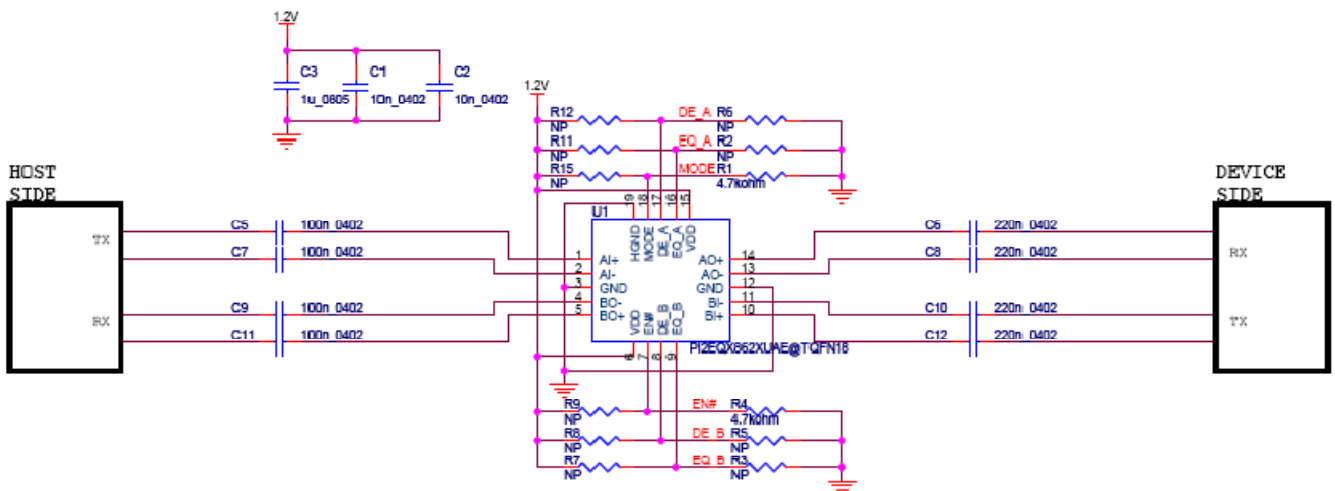

Figure 1: AC Coupling Capacitors between Host Chipset and PI2EQX862XUAE

2.2 External Pull-up/-down Resistors on all the control pins

There're total six external control pins of PI2EQX862XUAE, EQ_A/B, DE_A/B, Mode and EN# pins. And external resistor value is suggested to at least 4.7kohm for pull-up/-down selection in Figure2.
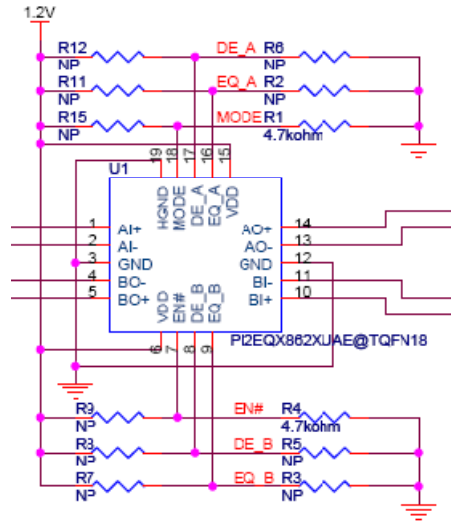
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Figure 2: Pull-up/down Resistors on external control pins.

3   Pin function description

3.1   Mode and EN#

Combination of Mode and EN# pins are for selection of SATA or PCIE function based on Table1 below.

EN#	MODE	MODE
0	0	SATA Application
0	1	PCIe Application
1	X	Disable

Table 1: Combination of Mode and EN# pins of PI2EQX862XUAE

Mode and EN# pins are internal High-Z impedance, so user should pull up/down by external resistors for selection.

3.2   EQ_A and EQ_B

EQ_A and EQ_B pins are tri-level input with internal 100kohm pull-up/-down resistors. They are effective for SATA and PCIE function. Table2 is available setting for input equalization of PI2EQX862XUAE.

Equalizer setting		
EQ_A/B	@3GHz	@4GHz
0	7dB	8dB
open	4dB (default)	5dB (default)
1	10dB	11dB

Table 2: Setting of EQ_A/B pins of PI2EQX862XUAE

3.3   DE_A and DE_B

DE_A and DE_B pins are tri-level input with internal 100kohm pull-up/-down resistors. **They are effective for PCIE only**. Table2 is available setting for output de-emphasis of PI2EQX862XUAE.

Output DE-Emphasis Setting	
DE	DE-Emphasis
0	-2.5 dB
open	0dB (Default)
1	-4dB

Table 3: Setting of DE_A/B pins of PI2EQX862XUAE

4   Layout Design Guideline

Layout guideline especially for high-speed transmission is highlighted.

4.1   Power and GROUND

To provide a clean power supply for PI2EQX862XUAE, few recommendations are listed below.
- ✓ Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly. The distance from each VDD or GND pin to the plane should be less than 50mil.
- ✓ The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- ✓ One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Smaller body size capacitors can facilitate component placement. The capacitor should be placed next to a VDD pin, i.e. within 100mil.
- ✓ One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- ✓ A ferrite bead for isolating the power supply for Pericom device and power supplies for other parts of the printed circuit board should also be implemented.

4.2   High-speed Signal Routing

As data rate is getting higher, good layout is essential to prevent signal from reflection.
- ✓ Differential impedance should follow SATA or PCIE spec requirement as 85~115ohm.
- ✓ Differential pair should maintain symmetrical routing whenever possible. **The intra-pair skew should be less than 5 mils**.
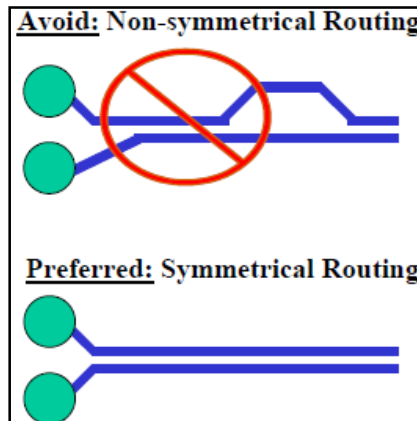
Figure 3: Layout Example of Differential Pair

- ✓ Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing.
- ✓ For minimal coupling, isolation spacing between two differential pairs should be maximized. At least 3 times the spacing of one differential pair is recommended.
- ✓ Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- ✓ It is preferable to route differential signals on the same layer of the printed circuit board, particularly for the input traces in source application.
- ✓ Stub creation should be avoided when placing shunt resistors on a differential pair.
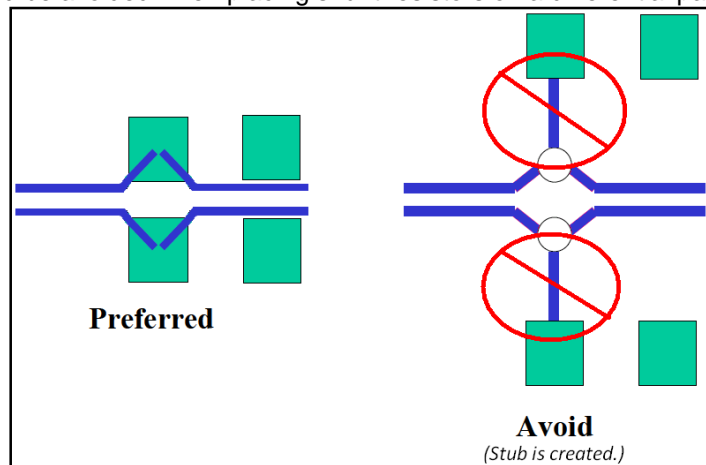
Figure 4: Shunt Resistor Placement

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✓ To minimize signal loss and jitter, tight bend is not recommended. All angles should be larger than or equal to 135 degrees.
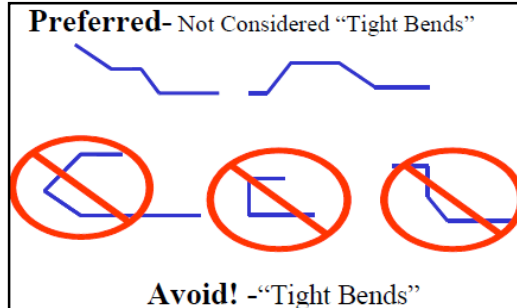

Figure 5: Acceptable Bends vs. Tight Bends

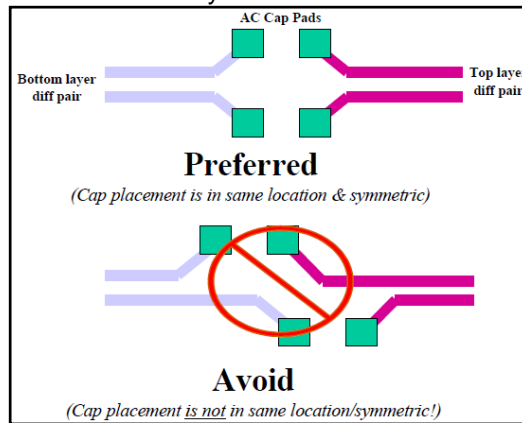✓ AC coupling capacitor placement should be symmetrical.

Figure 6: AC Capacitor Placement

✓ The use of vias should be avoided if possible. If using vias is a must, they should be used sparingly and must be placed symmetrically on a differential pair.
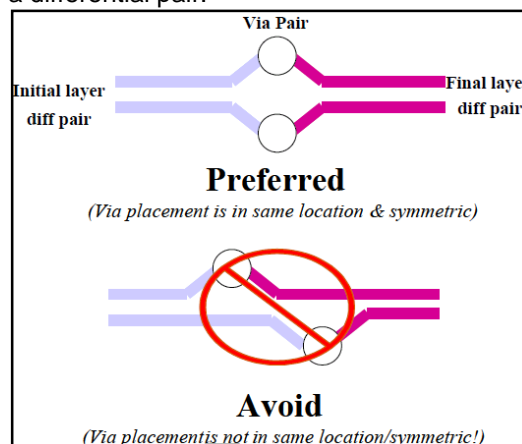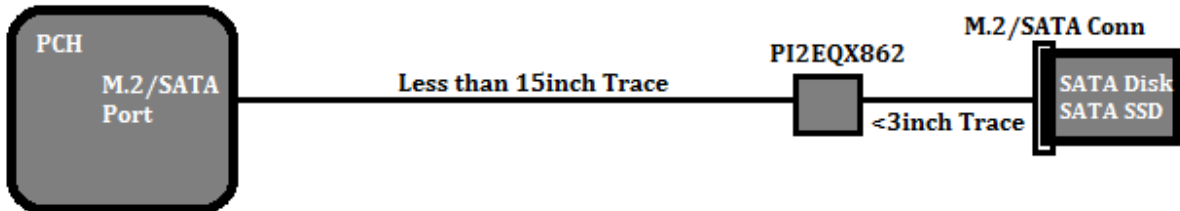

Figure 7: Via Placement

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4.3 PI2EQX862 Location in Layout

1, PI2EQX862 Location for M.2 SATA or SATA Express Application

PI2EQX862 layout location is suggested at less than 3inch trace to M.2 or SATA connector. And the trace length between PCH/HOST and PI2EQX862 is better to no longer than 15inch.

2, PI2EQX862 Location for M.2 PCIE Gen3/SATA Application

PI2EQX862 layout location is suggested at less than 3inch trace to M.2 connector. And the trace length between PCH/HOST and PI2EQX862 is better to no longer than 8inch because this is limited by PCIE Gen3 lane training pattern.
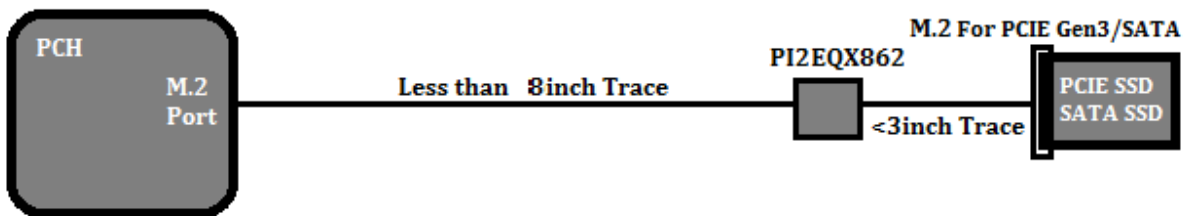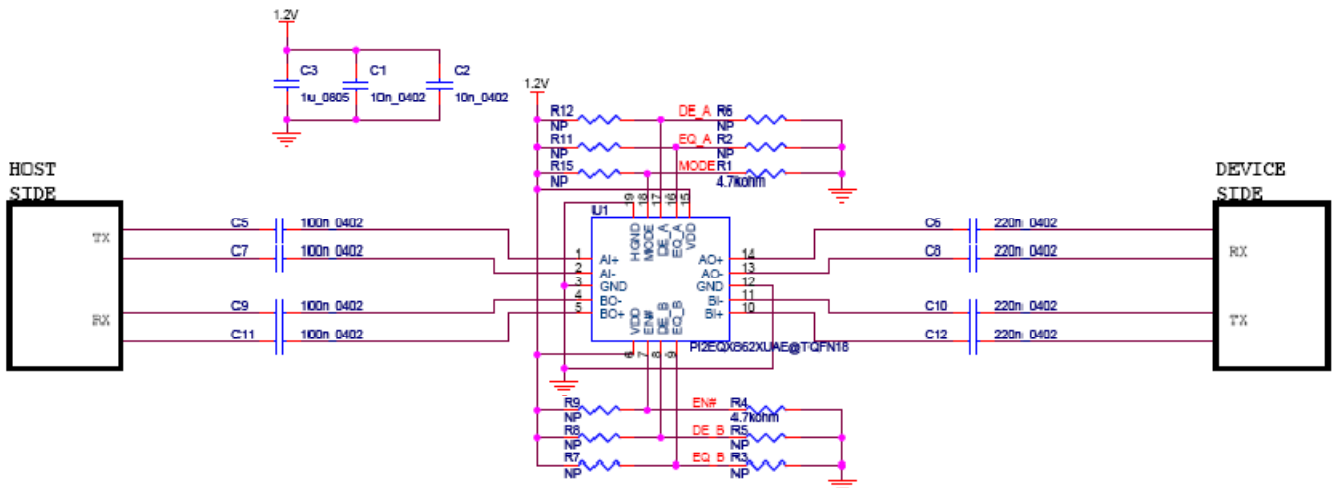
5 Typical Application Circuit

Figure 8: PI2EQX862XUAE Typical Application Circuit

6 Relative References

(1) Serial ATA Revision 3.2 Gold version, August 7, 2013
(2) PCIe_M.2_Electromechanical_Spec_Rev1.0_Final, November 1, 2013
(3) PCI Express Board Design Guidelines Draft, Intel Corporation, June 2003